TDA9955HL

Triple 8-bit analog-to-digital video converter for HDTV

Rev. 01 — 17 March 2008 Product data sheet

1. General description

The TDA9955HL is a triple 8-bit video converter interface.

The TDA9955HL converts an RGB analog signal into a RGB or YUV (YC_BC_R) digital signal or converts a YUV (YP_BP_R) analog signal into a YUV (YC_BC_R) or RGB digital signal with a sampling rate up to 170 MHz.

The TDA9955HL supports analog TV resolutions from 480i (720 × 480i at 60 Hz) to High-Definition TV (HDTV) (up to 1920 × 1080p at 60 Hz) and analog PC resolutions from VGA (640 × 480p at 60 Hz) to UXGA (1600 × 1200p at 60 Hz).

The YUV digital output signal can be 4 : 4 : 4 or 4 : 2 : 2 ITU-R BT.656 standard or semi-planar format following the ITU-R BT.601 standard.

All settings are controlled via the I^2C-bus.

2. Features

- Triple 8-bit Analog-to-Digital Converter (ADC)
- Three independent analog video sources, up to 170 MHz selectable via the I^2C-bus
- Analog composite sync slicer and recognition integrated
- Frame and field detection for interlaced video signal
- Video analog voltage input from 0.45 V to 0.9 V (p-p) to produce a full-scale ADC input of 1.0 V (p-p)
- Three clamps for programming a 8-bit clamping code from 0 to +191 in steps of 1 LSB for RGB and YUV signals
- Three video amplifiers controlled via I^2C-bus to reach the full-scale resolution
- Amplifier bandwidth of 100 MHz
- Low gain variation with temperature
- I^2C-bus controlled Phase-Locked Loop (PLL) to generate the ADCs, formatter and output clocks which can be locked into a line frequency from 15 kHz to 95 kHz
- Integrated PLL divider
- Programmable clock phase adjustment cells
- Matrix and offsets available for conversion of RGB or YUV signal coming from analog video sources into YUV or RGB
- Output format RGB 4 : 4 : 4, YUV 4 : 4 : 4, YUV 4 : 2 : 2 ITU-R BT.656 or YUV 4 : 2 : 2 semi-planar standard on output bus
- Integrated downsampling-by-two with selectable filters on C_B and C_R channels in the 4 : 2 : 2 mode
- IC controlled via the I^2C-bus, 5 V tolerant and bit rate up to 400 kbit/s

founded by Philips

- TTL inputs 5 V tolerant
- LV-TTL outputs
- Power-down mode
- 1.8 V and 3.3 V power supplies

3. Applications

- Set Top Box (STB)
- YUV or RGB high-speed video digitizer
- Projector, plasma and LCD TV
- Rear projection TV
- High-end TV

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TDA9955HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

5. Block diagram

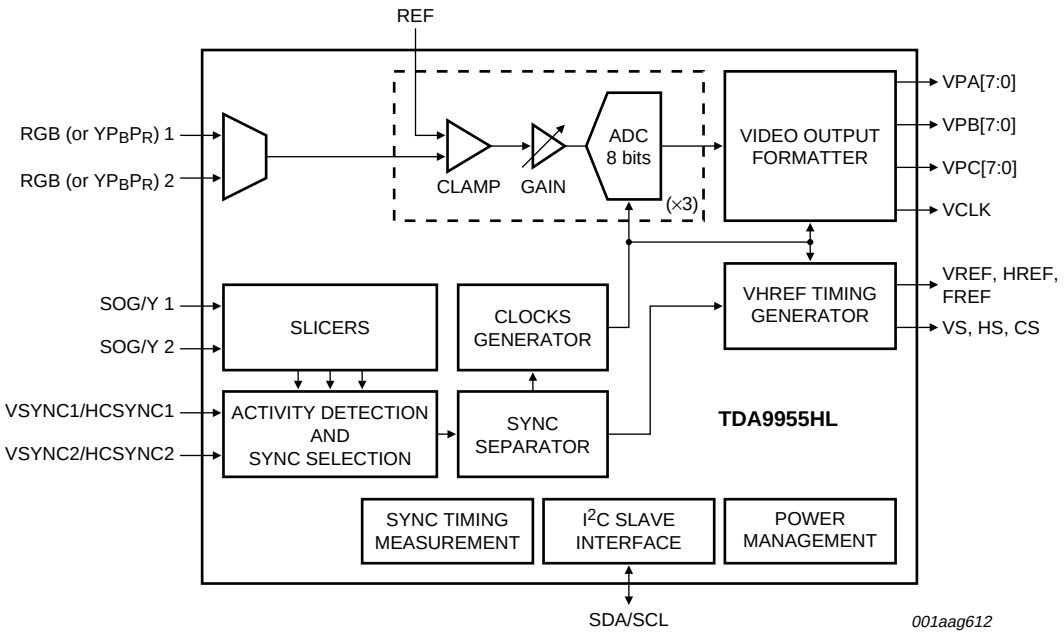


Fig 1. Block diagram

© NXP B.V. 2008. All rights reserved.

6. Functional diagram

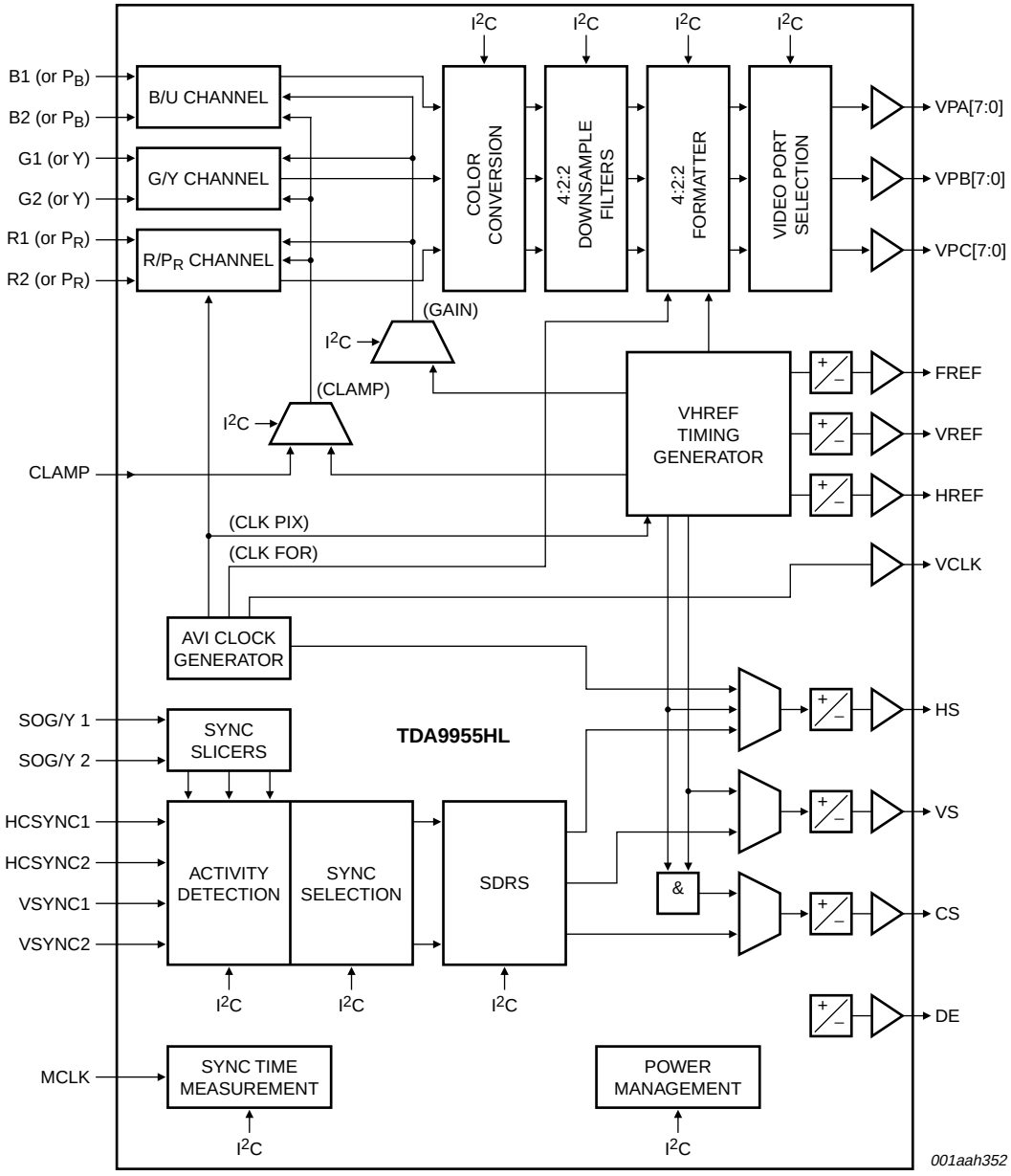


Fig 2. Functional diagram

© NXP B.V. 2008. All rights reserved.

7. Pinning information

7.1 Pinning

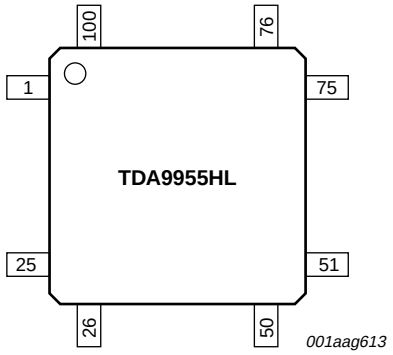


Fig 3. Pin configuration

7.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
VPC1	1	O	video port C output bit 1
VPC2	2	O	video port C output bit 2
VPC3	3	O	video port C output bit 3
$V_{DDC(1V8)}$	4	P	supply voltage for the digital core (1.8 V)
V_{SSC}	5	G	ground for the digital core
$V_{DDO(3V3)}$	6	P	supply voltage for the video port output (3.3 V)
V_{SSO}	7	G	ground for the video port output
VPC4	8	O	video port C output bit 4
VPC5	9	O	video port C output bit 5
VPC6	10	O	video port C output bit 6
VPC7	11	O	video port C output bit 7
$V_{DDO(3V3)}$	12	P	supply voltage for the video port output (3.3 V)
V_{SSO}	13	G	ground for the video port output
VCLK	14	O	pixel clock output
FREF/CS	15	O	filed reference output or composite synchronization
VREF/VS	16	O	vertical reference output or vertical synchronization
HREF/HS	17	O	horizontal reference output or horizontal synchronization
DE	18	O	data enable signal output
VAI_N	19	O	video activity indication output (active LOW)
$V_{DDA(OSC)(3V3)}$	20	P	analog supply for the free running oscillator (3.3 V)
$V_{SSA(OSC)}$	21	G	analog ground for the free running oscillator
$V_{DDA(BIAS)(3V3)}$	22	P	bias analog supply voltage (3.3 V)
$V_{SSA(BIAS)}$	23	G	bias analog ground

© NXP B.V. 2008. All rights reserved.

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
BIAS	24	I	bias input
V_{SSA}	25	G	PCB ground
$V_{SSA(B)}$	26	G	analog ground for the blue (or blue chrominance) channel
$V_{DDA(B)(3V3)}$	27	P	analog supply voltage for blue (or blue chrominance) channel (3.3 V)
B2	28	I	blue channel input 2
REF_B	29	I	blue channel reference input
B1	30	I	blue channel input 1
$V_{DDA(B)(1V8)}$	31	P	analog supply voltage for blue (or blue chrominance) channel ADC (1.8 V)
$V_{SSA(B)}$	32	G	analog ground for blue (or blue chrominance) channel ADC
$V_{SSA(G)}$	33	G	analog ground for green (or green luminance) channel
$V_{DDA(G)(3V3)}$	34	P	analog supply voltage for green (or green luminance) channel (3.3 V)
G2	35	I	green channel input 2
REF_G	36	I	green channel reference input
G1	37	I	green channel input 1
$V_{DDA(G)(1V8)}$	38	P	analog supply voltage for green (or green luminance) channel ADC (1.8 V)
$V_{SSA(G)}$	39	G	analog ground for green (or green luminance) channel ADC
$V_{SSA(R)}$	40	G	analog ground for red (or red chrominance) channel
$V_{DDA(R)(3V3)}$	41	P	analog supply voltage for red (or red chrominance) channel (3.3 V)
R2	42	I	red channel input 2
REF_R	43	I	red channel reference input
R1	44	I	red channel input 1
$V_{DDA(R)(1V8)}$	45	P	analog supply voltage for red (or red chrominance) channel ADC (1.8 V)
$V_{SSA(R)}$	46	G	analog ground for red (or red chrominance) channel ADC
SOG2	47	I	Sync-On-Green (SOG) input 2
SOG1	48	I	sync-on-green input 1
$V_{DDA(SOG)(3V3)}$	49	P	analog supply voltage for SOG (3.3 V)
$V_{SSA(SOG)}$	50	G	analog ground for SOG
$V_{DDA(SOG)(3V3)}$	51	P	analog supply voltage for SOG (3.3 V)
$V_{SSA(SOG)}$	52	G	analog ground for SOG
$V_{SSA(PLL)}$	53	G	analog ground for PLL
$V_{SSA(PLL)}$	54	G	analog ground for PLL
$V_{DDA(PLL)(3V3)}$	55	P	analog supply voltage for PLL (3.3 V)
$V_{DDA(PLL)(1V8)}$	56	P	analog supply voltage for PLL (1.8 V)
TEST0	57	I	reserved for test (connected to the digital ground of the core)
TEST1	58	I	reserved for test (connected to the digital ground of the core)
HCSYNC1	59	I	horizontal (composite) SYNC input 1
HCSYNC2	60	I	horizontal (composite) SYNC input 2

© NXP B.V. 2008. All rights reserved.

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
VSYNC1	61	I	vertical SYNC input 1
VSYNC2	62	I	vertical SYNC input 2
MCLK	63	I	synchronization timing measurement clock
CLAMP	64	I	clamp input (external mode)
COAST	65	I	coast (PLL) input (external mode)
CKEXT	66	I	external clock input (external mode)
A0	67	I	I^2C-bus address select bit 0
$V_{DDI(3V3)}$	68	P	digital supply for the input (3.3 V)
SCL	69	I	I^2C-bus clock
SDA	70	I	I^2C-bus data
V_{SSA}	71	G	analog ground
$V_{DDC(1V8)}$	72	P	digital supply for core (1.8 V)
V_{SSC}	73	G	digital ground of the core (1.8 V)
$V_{DDO(3V3)}$	74	P	supply voltage for the video port output (3.3 V)
V_{SSO}	75	G	ground for video port output
VPA0	76	O	video port A output bit 0
VPA1	77	O	video port A output bit 1
VPA2	78	O	video port A output bit 2
VPA3	79	O	video port A output bit 3
$V_{DDO(3V3)}$	80	P	supply voltage for the video port output (3.3 V)
V_{SSO}	81	G	ground for video port output
VPA4	82	O	video port A output bit 4
VPA5	83	O	video port A output bit 5
VPA6	84	O	video port A output bit 6
VPA7	85	O	video port A output bit 7
$V_{DDO(3V3)}$	86	P	supply voltage for the video port output (3.3 V)
V_{SSO}	87	G	ground for video port output
VPB0	88	O	video port output bit 0
VPB1	89	O	video port output bit 1
VPB2	90	O	video port output bit 2
VPB3	91	O	video port output bit 3
$V_{DDO(3V3)}$	92	P	supply voltage for the video port output (3.3 V)
V_{SSO}	93	G	ground for video port output
VPB4	94	O	video port output bit 4
VPB5	95	O	video port output bit 5
VPB6	96	O	video port output bit 6
VPB7	97	O	video port output bit 7
$V_{DDO(3V3)}$	98	P	supply voltage for the video port output (3.3 V)
V_{SSO}	99	G	ground for video port output
VPC0	100	O	video port C output bit 0

[1] P = power supply; G = ground; I = input and O = output.

© NXP B.V. 2008. All rights reserved.

8. Functional description

This high-rate front end is designed to convert analog signals coming from an analog source (RGB or YUV) into parallel digital data used by media processor ICs such as the NXP Semiconductors Nexperia devices for HDTV or by other video signal ICs. The high-rate front end is able to output RGB 4 : 4 : 4, YUV 4 : 4 : 4, YUV 4 : 2 : 2 semi-planar and YUV 4 : 2 : 2 ITU-R BT.656 formats and accepts progressive and interlaced input formats. The high-rate front end also contains a RGB-to-YUV and YUV-to-RGB conversion matrix, downsampling filters and range control function.

8.1 Analog multiplexers

The choice between the two analog video inputs is either automatic (activity detection) or controlled by the I^2C-bus. An analog video input is defined by pins SOGx, Rx, Bx, Gx, HCSYNCx and VSYNCx (where x equals 1 or 2).

8.2 R/P_R, B/P_B and G/Y channels

8.2.1 Clamps

Three independent parallel clamping circuits are used to clamp the video input signals on programmable black/blanking levels. The clamp level of each channel can be changed from 0 to 191 in steps of 1 LSB. The clamp signal comes from the VHREF timing generator or from the CLAMP pin.

The clamping circuits can be inhibited during the vertical sync pulse and also during false black/blanking level in the end of active video signal in a frame/field.

8.2.2 ADCs

Three ADCs convert analog signals into three series of 8-bit codes, with a maximum sampling frequency of 170 MHz. The ADCs input range is 1 V (p-p).

During the gain calibration pulse period, the ADCs are used to calibrate the video amplifiers and during the clamp active period the ADCs are used to set the clamp level to the desired values.

8.2.3 Automatic Gain Control (AGC)

Gain registers, one per channel, control directly the gain of each video amplifier. The programming of these registers is done by I^2C-bus and their content is validated only on the next horizontal synchronization pulse. These contrast registers are programmable from 0 dB to 5 dB (gain registers on 11 bits).

The gain calibration control signal comes from the VHREF timing generator.

8.3 Sync slicing

Two sync slicers extract the composite sync from the green, luminance or CVBS signal through SOGx pins. This synchronization signal can be bi-level or tri-level.

© NXP B.V. 2008. All rights reserved.

8.4 Activity detection

The device detects the presence of signals on each sync input VSYNCx, HCSYNCx and SOGx after slicing to indicate which kind of synchronization is present (where x equals 1 or 2):

- Digital separated syncs on VSYNCx and HCSYNCx
- Analog composite sync on SOGx

A change of activity is notified by a HIGH-to-LOW transition on the VAI_N output pin.

8.5 Sync detection and selection

The management of the synchronization is done by using vertical sync, horizontal sync and analog composite sync on the green/luminance signal.

The device scans if a signal is present on the VSYNCx pin. If a signal is detected on this pin, it means that there is a digital separated sync signal.

If no signal is detected on the HCSYNCx pin, the device scans if a signal is present on the SOGx pin. If a signal is detected on this pin (and not on the HCSYNCx pin), it means that there is an analog composite sync signal and the signal is sent into the sync recognition function after slicing.

If the analog composite sync signal is on the green or on the luminance of the video signal, the SOGx pin must be connected to this signal.

8.6 Sync Detection Recognition and Separation

The Sync Detection Recognition and Separation (SDRS) allows to retrieve the horizontal and the vertical synchronizations from composite sync. This composite sync comes from the sync slicing function when the sync is on the green, luminance or CVBS signal or from the digital composite sync on the HCSYNCx pin.

This function is able to eliminate any additional synchronization pulses which may be added in the vertical blanking.

8.7 Clock generator

An internal PLL locked to the reference HSYNC signal from sync recognition provides three different clocks, one pixel-clock for R/P_R, B/P_B and G/Y channels sampling and for the VHREF timing generator, one formatter-clock at double frequency for the 4 : 2 : 2 formatter and one output-clock for the VCLK output pin.

The COAST signal, coming from SDRS and/or VHREF timing generator or coming from the COAST input pin, allows to freeze the PLL phase frequency detector during the vertical blanking.

A phase-locked flag indicates if the PLL is locked.

8.8 Sync multiplexers

The sync multiplexer allow to select via the I^2C-bus the origin of the synchronization pulses signals HS, VS, CS and DE.

© NXP B.V. 2008. All rights reserved.

The origin of those pulses can be the VHREF timing generator or the SDRS block.

8.9 Color conversion

The color conversion allows an RGB signal coming from the analog video interface to convert into YUV format or to convert a YUV signal coming from the analog video interface into an RGB format. The color matrix formula is:

$$\begin{bmatrix} YG \\ VR \\ UB \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \times \left(\begin{bmatrix} GY \\ RV \\ BU \end{bmatrix} - \begin{bmatrix} Oin_1 \\ Oin_2 \\ Oin_3 \end{bmatrix} \right) + \begin{bmatrix} Oout_1 \\ Oout_2 \\ Oout_3 \end{bmatrix}$$

Activation of the matrix function and programming of all coefficients is made by I^2C-bus.

8.10 4 : 2 : 2 downsample filters

These filters downsample the U and V signals with a factor 2.

A delay is added on the G/Y channel corresponding to the pipeline delay of the filters to put the Y channel in phase with the UV channel.

Four filters are selectable by I^2C-bus, from the simple cut to the ITU-R BT.656 compliant digital filter.

8.11 Range control

The range control function truncates the range of data at specified ceiling and floor values to remove super-white and super-black pixels.

8.12 4 : 2 : 2 formatter

The 4 : 2 : 2 formatter contains the YUV 4 : 2 : 2 semi-planar and the YUV 4 : 2 : 2 ITU-R BT.656 formatting functions. The choice between these functions is done using the I^2C-bus. A delay is added on the G/Y channel corresponding to the pipeline delay of the YUV 4 : 2 : 2 semi-planar formatting function to put the Y channel in phase with the UV channel.

In the case of the YUV 4 : 2 : 2, the data frequency corresponding to the Y signal is at pixel clock frequency and the data frequency corresponding to the U and V signals is at half the pixel clock frequency. For semi-planar, the output clock should be at the same frequency as the pixel clock and for ITU-R BT.656 at the same frequency as the formatter clock (double of the pixel-clock).

The Start Active Video (SAV) and End Active Video (EAV) timing reference codes can be included in the data stream according the HREF, VREF and FREF signal positions from the VHREF timing generator.

Specific codes programmed via the I^2C-bus can replace the data stream during the blanking period to mask gain and clamp calibration.

© NXP B.V. 2008. All rights reserved.

8.13 Video port selection

Each channel (R or G or B in RGB 4 : 4 : 4 mode, Y or C_B or C_R in YUV 4 : 4 : 4 mode, Y or C_BC_R in 4 : 2 : 2 semi-planar mode, C_BYC_RY in 4 : 2 : 2 ITU-R BT.656 mode) can be affected to a specified video port VPA, VPB or VPC via the I²C-bus.

8.14 Output buffers

The levels of the output buffers are LV-TTL compatible. The switch of the outputs between active and high-impedance is set by the I²C-bus.

8.15 VHREF timing generator

The VHREF timing generator outputs all the timing signals used by the device: gain and clamp pulses for calibration, coast signal to manage the PLL, VREF, HREF and FREF signals for SAV/EAV and other, VS and HS signals to change width and position compared with the synchronization inputs.

8.16 I²C-bus serial interface

The I²C-bus serial interface allows to program the internal registers of the device. The slave address of the device is selected by pin A0. The programmed values in the registers remain valid.

8.17 Power management

Only the serial interface (and the I²C-bus registers) and the activity detection are powered up in all cases even in the case when the device is set to power-down with the PD-registers.

8.18 Sync timing measurement

To assist the recognition of the input format, the vertical and horizontal periods are measured based on the externally provided MCLK frequency (13.5 MHz). The width of the horizontal pulse is also measured.

9. I²C-bus interface

9.1 I²C-bus protocol

The TDA9955HL is a slave I²C-bus device and the SCL pin is only an input pin. The timing and protocol for I²C-bus are standard.

Bit A0 of the I²C-bus device address is externally selected by the A0 pin. The main device I²C-bus address is given in Table 3.

Table 3. I²C-bus slave address

Device address							R/$\overline{W}$
A6	A5	A4	A3	A2	A1	A0	-
1	0	0	1	1	1	A0	0/1

© NXP B.V. 2008. All rights reserved.

9.2 Registers definitions

The configuration of the registers is given in Table 4.

Table 4. I²C-bus registers; (R): reading register[1]

Register	Sub addr	R/W	Bit definition								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
VERSION	00h	R	0	0	0	1	0	1	0	0	0001 0100
INPUT_SEL	01h	W	x	x	x	x	x	x	VINS[1:0]		0000 0100
Reserved for test	02h	W	-	-	x	x	x	-	x	x	0000 0000
Reserved for test	03h	W	x	x	x	x	x	x	x	x	0110 0000
SDRS_CTRL1	04h	W	x	ASD_DIS	SOGF	DCSF	x	x	x	x	0000 0000
Reserved for test	05h	W	x	x	x	x	x	x	x	x	0000 0010
Reserved for test	06h	W	x	x	x	x	x	x	x	x	0001 0100
Reserved for test	07h	W	x	x	x	x	x	x	x	x	0001 0000
Reserved for test	08h	W	x	x	x	x	x	x	x	x	0000 0000
Reserved for test	09h	W	x	x	x	x	x	x	x	x	0111 1111
Reserved for test	0Ah	W	x	x	x	x	x	x	x	x	0010 0101
Reserved for test	0Bh	R	-	-	-	x	x	x	x	x	0000 0000
Reserved for test	0Ch	R	x	x	x	x	x	x	x	x	0000 0000
SDRS_FLAGS	0Dh	R	ASD	SOGD2	-	DSSD2	-	SOGD1	-	DSSD1	0000 0000
PLL_CTRL	10h	W	x	-	-	-	EDG	x	x	x	0000 0000
PLL_MNDIV_MSB	11h	W	MDIV[1:0]		-	-	NDIV[11:8]				1100 0011
PLL_NDIV_LSB	12h	W	NDIV[7:0]								0110 0000
LOCK_FLAG	13h	R	-	-	-	-	-	-	x	PLL_LOCK	0000 0000
DLL_PHASE	14h	W	-	-	-	PHASE[4:0]					0001 0000
PIXCLKGEN_PRST	15h	W	CLKOUT_PRST[2:0]			CLKFOR_PRST[1:0]		CLKPIX_PRST[2:0]			1101 0111
PIXCLKGEN_CTRL0	16h	W	CLKOUT_DIV[1:0]		CLKFOR_DIV[1:0]		CLKPIX_DIV[1:0]		PR_DEL	PH_CORR	0011 1011
PIXCLKGEN_CTRL1	17h	W	CLKOUT_TOG	CLKOUT_SEL[2:0]			CLKFOR_SEL[1:0]		x	x	0100 0110
BRIGHT_GY	1Ah	W	BRIGHT_GY[7:0]								0001 0000
BRIGHT_BU	1Bh	W	BRIGHT_BU[7:0]								1000 0000
BRIGHT_RV	1Ch	W	BRIGHT_RV[7:0]								1000 0000
Reserved for test	1Dh	W	x	x	x	x	x	x	x	x	0000 0000
Reserved for test	1Eh	W	-	-	-	-	-	x	x	x	0000 0000

© NXP B.V. 2008. All rights reserved.

Table 4. I²C-bus registers; (R): reading register[1] *…continued*

Register	Sub addr	R/W	Bit definition								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
COARSE_GAINRV	20h	W	-	-	-	-	COARSE_RV[3:0]				0000 0100
FINE_GAINRV	21h	W	-	FINE_RV[6:0]							0101 1100
AGC_HIGHRV	22h	W	HIGH_RV[7:0]								1111 0000
AGC_LOWRV	23h	W	x	LOW_RV[6:0]							1001 0000
COARSE_GAINBU	2Ah	W	-	-	-	-	COARSE_BU[3:0]				0000 0100
FINE_GAINBU	2Bh	W	-	FINE_BU[6:0]							0101 1100
AGC_HIGHBU	2Ch	W	HIGH_BU[7:0]								1111 0000
AGC_LOWBU	2Dh	W	x	LOW_BU[6:0]							1001 0000
AGC_CONTGY	34h	W	-	-	-	-	COARSE_GY[3:0]				0000 0100
AGC_OFFSETGY	35h	W	-	FINE_GY[6:0]							0101 1100
AGC_HIGHGY	36h	W	HIGH_GY[7:0]								1110 1011
AGC_LOWGY	37h	W	x	LOW_GY[6:0]							1001 0000
V_PER_MSB	40h	R	V_PER[19:12]								0000 0000
V_PER_ISB	41h	R	V_PER[11:4]								0000 0000
H_PER_MSB	42h	R	H_PER[9:2]								0000 0000
HS_WIDTH_MSB	43h	R	HS_WIDTH[9:2]								0000 0000
STM_LSB	44h	R	V_PER[3:0]				H_PER[1:0]		HS_WIDTH[1:0]		0000 0000
MAT_CTRL	80h	W	-	-	-	-	-	-	MAT_SC[1:0]		0000 0010
MAT_OI1_MSB	81h	W	-	-	-	-	-	MAT_OI1[8:6]			0000 0000
MAT_OI1_LSB	82h	W	OFFSET_IN1[5:0]						-	-	0000 0000
MAT_OI2_MSB	83h	W	-	-	-	-	-	MAT_OI2[8:6]			0000 0000
MAT_OI2_LSB	84h	W	OFFSET_IN2[5:0]						-	-	0000 0000
MAT_OI3_MSB	85h	W	-	-	-	-	-	MAT_OI3[8:6]			0000 0000
MAT_OI3_LSB	86h	W	OFFSET_IN3[5:0]						-	-	0000 0000
MAT_P11_MSB	87h	W	-	-	-	-	-	P11[10:8]			0000 0000
MAT_P11_LSB	88h	W	P11[7:0]								0000 0010
MAT_P12_MSB	89h	W	-	-	-	-	-	P12[10:8]			0000 0001
MAT_P12_LSB	8Ah	W	P12[7:0]								0000 0110
MAT_P13_MSB	8Bh	W	-	-	-	-	-	P13[10:8]			0000 0000
MAT_P13_LSB	8Ch	W	P13[7:0]								0110 0100

© NXP B.V. 2008. All rights reserved.

Table 4. I²C-bus registers; (R): reading register[1] *…continued*

Register	Sub addr	R/W	Bit definition								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
MAT_P21_MSB	8Dh	W	-	-	-	-	-	P21[10:8]			0000 0110
MAT_P21_LSB	8Eh	W	P21[7:0]								1000 1001
MAT_P22_MSB	8Fh	W	-	-	-	-	-	P22[10:8]			0000 0001
MAT_P22_LSB	90h	W	P22[7:0]								1100 0000
MAT_P23_MSB	91h	W	-	-	-	-	-	P23[10:8]			0000 0111
MAT_P23_LSB	92h	W	P23[7:0]								1011 0111
MAT_P31_MSB	93h	W	-	-	-	-	-	P31[10:8]			0000 0110
MAT_P31_LSB	94h	W	P31[7:0]						-	-	1101 0111
MAT_P32_MSB	95h	W	-	-	-	-	-	P32[10:8]			0000 0111
MAT_P32_LSB	96h	W	P32[7:0]						-	-	0110 1001
MAT_P33_MSB	97h	W	-	-	-	-	-	P33[10:8]			0000 0001
MAT_P33_LSB	98h	W	P33[7:0]						-	-	1100 0000
MAT_OO1_MSB	99h	W	-	-	-	-	-	OFFSET_OUT1[8:6]			0000 0000
MAT_OO1_LSB	9Ah	W	OFFSET_OUT1[5:0]						-	-	0100 0000
MAT_OO2_MSB	9Bh	W	-	-	-	-	-	OFFSET_OUT2[8:6]			0000 0010
MAT_OO2_LSB	9Ch	W	OFFSET_OUT2[5:0]						-	-	0000 0000
MAT_OO3_MSB	9Dh	W	-	-	-	-	-	OFFSET_OUT3[8:6]			0000 0010
MAT_OO3_LSB	9Eh	W	OFFSET_OUT3[5:0]						-	-	0000 0000
MAT_BYPASS	9Fh	W	-	-	-	-	-	-	-	MAT_BP	0000 0001
Reserved for test	A0h	W	x	x	x	x	x	x	x	x	0001 0000
PXCNT_PR_LSB	A1h	W	PXCNT_PR[7:0]								0000 0011
PXCNT_MSB	A2h	W	PXCNT_PR[11:8]					PXCNT_NPIX[11:8]			0000 0011
PXCNT_NPIX_LSB	A3h	W	PXCNT_NPIX[7:0]								0110 0000
LCNT_PR_LSB	A4h	W	LCNT_PR[7:0]								0000 0001
LCNT_MSB	A5h	W	LCNT_PR[11:8]					LCNT_NLIN[11:8]			0000 0000
LCNT_NLIN_LSB	A6h	W	PXCNT_NLIN[7:0]								0000 0000
HREF_S_LSB	A7h	W	HREF_START[7:0]								0000 0000
HREF_MSB	A8h	W	HREF_START[11:8]					HREF_END[11:8]			0000 0000
HREF_E_LSB	A9h	W	HREF_END[7:0]								0000 0000
HS_S_LSB	AAh	W	HS_START[7:0]								0000 0000

© NXP B.V. 2008. All rights reserved.

Table 4. I²C-bus registers; (R): reading register[1] *…continued*

Register	Sub addr	R/W	Bit definition								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
HS_MSB	ABh	W	HS_START[11:8]					HS_END[11:8]			0000 0000
HS_E_LSB	ACh	W	HS_END[7:0]								0000 0000
VREF_F1_S_MSB	ADh	W	-	-	-	-	-	VREF_F1_START[10:8]			0000 0000
VREF_F1_S_LSB	AEh	W	VREF_F1_START[7:0]								0000 0000
VREF_F1_WIDTH	AFh	W	VREF_F1_WIDTH[7:0]								0000 0000
VREF_F2_S_MSB	B0h	W	-	-	-	-	-	VREF_F2_START[10:8]			0000 0000
VREF_F2_S_LSB	B1h	W	VREF_F2_START[7:0]								0000 0000
VREF_F2_WIDTH	B2h	W	VREF_F2_WIDTH[7:0]								0000 0000
VS_F1_LINE_S_MSB	B3h	W	-	-	-	-	-	VS_F1_LINE_START[10:8]			0000 0000
VS_F1_LINE_S_LSB	B4h	W	VS_F1_LINE_START[7:0]								0000 0000
VS_F1_LINE_WIDTH	B5h	W	VS_F1_LINE_WIDTH[7:0]								0000 0000
VS_F2_LINE_S_MSB	B6h	W	-	-	-	-	-	VS_F2_LINE_START[10:8]			0000 0000
VS_F2_LINE_S_LSB	B7h	W	VS_F2_LINE_START[7:0]								0000 0000
VS_F2_LINE_WIDTH	B8h	W	VS_F2_LINE_WIDTH[7:0]								0000 0000
VS_F1_PIX_S_LSB	B9h	W	VS_F1_PIX_START[7:0]								0000 0001
VS_F1_PIX_MSB	BAh	W	VS_F1_PIX_START[11:8]					VS_F1_PIX_END[11:8]			0000 0000
VS_F1_PIX_E_LSB	BBh	W	VS_F1_PIX_END[7:0]								0000 0001
VS_F2_PIX_S_LSB	BCh	W	VS_F2_PIX_START[7:0]								0000 0001
VS_F2_PIX_MSB	BDh	W	VS_F2_PIX_START[11:8]					VS_F2_PIX_END[11:8]			0000 0000
VS_F2_PIX_E_LSB	BEh	W	VS_F2_PIX_END[7:0]								0000 0001
FREF_F1_S_LSB	BFh	W	FREF_F1_START[7:0]								0000 0000
FREF_POL_MSB	C0h	W	FPOL	FREF_F1_START[10:8]			-	FREF_F2_START[10:8]			0000 0000
FREF_F2_S_LSB	C1h	W	FREF_F2_START[7:0]								0000 0000
CLAMP_PIX_S_LSB	C8h	W	CLAMP_PIX_START[7:0]								0000 0000
CLAMP_PIX_MSB	C9h	W	CLAMP_PIX_START[11:8]					CLAMP_PIX_END[11:8]			0000 0000
CLAMP_PIX_E_LSB	CAh	W	CLAMP_PIX_END[7:0]								0000 0000
CLP_F1_LINE_S_MSB	CBh	W	-	-	-	-	-	CLAMP_F1_LINE_START[10:8]			0000 0000
CLP_F1_LINE_S_LSB	CCh	W	CLAMP_F1_LINE_START[7:0]								0000 0000
CLP_F1_LINE_WIDTH	CDh	W	CLAMP_F1_LINE_WIDTH[7:0]								0000 0000
CLP_F2_LINE_S_MSB	CEh	W	-	-	-	-	-	CLAMP_F2_LINE_START[10:8]			0000 0000

© NXP B.V. 2008. All rights reserved.

Table 4. I²C-bus registers; (R): reading register[1] *…continued*

Register	Sub addr	R/W	Bit definition								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
CLP_F2_LINE_S_LSB	CFh	W	CLAMP_F2_LINE_START[7:0]								0000 0000
CLP_F2_LINE_WIDTH	D0h	W	CLAMP_F2_LINE_WIDTH[7:0]								0000 0000
GAIN_S_LSB	D1h	W	GAIN_START[7:0]								0000 0001
GAIN_MSB	D2h	W	GAIN_START[11:8]				GAIN_END[11:8]				0000 0000
GAIN_E_LSB	D3h	W	GAIN_END[7:0]								0101 0001
FDW_S_LSB	D4h	W	FDW_START[7:0]								0000 0000
FDW_MSB	D5h	W	FDW_START[11:8]				FDW_END[11:8]				0000 0000
FDW_E_LSB	D6h	W	FDW_END[7:0]								0000 0000
ASD_MEASLIN_MSB	D7h	R	x	x	x	x	x	MEAS_LINES[10:8]			0000 0000
MEASLIN_LSB	D8h	R	MEAS_LINES[7:0]								0000 0000
MEASPIX_MSB	D9h	R	-	-	-	-	MEAS_PIX[11:8]				0000 0000
MEASPIX_LSB	DAh	R	MEAS_PIX[7:0]								0000 0000
Reserved for test	DBh	W	x	x	x	x	x	x	x	x	0000 0000
BLK_GY_LSB	DCh	W	BLK_GY[5:0]						-	-	0100 0000
BLK_BU_LSB	DDh	W	BLK_BU[5:0]						-	-	0000 0000
BLK_RV_LSB	DEh	W	BLK_RV[5:0]						-	-	0000 0000
BLK_MSB	DFh	W	BLK_GY[7:6]		-	BLK_BU[7:6]		-	BLK_RV[7:6]		0001 0010
PRE_FILTERS	E0h	W	-	-	FILTERBU[1:0]		-	-	FILTERRV[1:0]		0010 0010
OF_CCEIL	E1h	W	-	-	C_CEIL[5:0]						1100 0000
OF_CFLOOR	E2h	W	-	-	C_FLOOR[5:0]						0100 0000
OF_YCEIL	E3h	W	-	-	Y_CEIL[5:0]						1010 1100
OF_YFLOOR	E4h	W	-	-	Y_FLOOR[5:0]						0100 0000
OF_CTRL	E5h	W	OUT	VPL	-	BLC	TRC	-	FOR_SEL[1:0]		0100 0010
Reserved for test	E6h	W	x	x	x	x	x	x	x	x	0000 0001
Reserved for test	E7h	W	-	-	-	-	x	x	x	x	0000 0000
CSVSHS_SEL	E8h	W	CS_SEL[2:0]			VS_SEL[1:0]		HS_SEL[2:0]			0000 0000
POL_CTRL	E9h	W	-	-	CS_POL	HS_POL	VS_POL	FREF_POL	HREF_POL	VREF_POL	0000 0000
OUTPUT_CTRL	EAh	W	-	-	VPC_SEL[1:0]		VPB_SEL[1:0]		VPA_SEL[1:0]		1010 0100
DE_CNTRL	EBh	W	HR_PXQ	HR_SEL	DE_PXQ	DE_POL	-	-	-	-	0000 1000
RESET_CNTRL	F1h	W	-	-	-	RST_MAN	RST_AVI	-	-	-	0000 0101

© NXP B.V. 2008. All rights reserved.

Table 4. I²C-bus registers; (R): reading register[1] *…continued*

Register	Sub addr	R/W	Bit definition								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
PD_AVI_CNTRL0	F4h	W	-	-	-	PD_SOG2	PD_SOG1	PD_DLL	PD_PLL	PD_AVI	0000 0000
PD_AVI_CNTRL1	F5h	W	-	-	-	-	-	PD_ADC_B	PD_ADC_G	PD_ADC_R	0010 0000
FVH_SEL	F6h	W	-	-	-	-	-	-	-	FVH_SEL	0000 0001
LSB_OUT_SEL	F7h	W	LSB_SEL[7:0]								0000 0000
OR_SEL	F9h	W	x	x	x	x	x	x	x	x	0000 0000

[1] The symbol ‘x’ indicates a bit reserved for test and the symbol ‘-’ indicates that the bit is not used.

© NXP B.V. 2008. All rights reserved.

9.2.1 Version register

Table 5. VERSION register (address 00h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 0	-	R	14h*	the version register gives the version of the device, version is 0001 0100

9.2.2 Input selection register

Table 6. INPUT_SEL register (address 01h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 2	x	W	00 0001*	for test: must be set to default value for proper operation
1 to 0	VINS[1:0]	W		**video input selection:** enables analog video input 1, analog video input 2
			00*	video input 1
			01	video input 2

9.2.3 Sync detection recognition and separation registers

Table 7. SDRS_CTRL1 register (address 04h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	x	R/W	0*	for test: must be set to default value for proper operation
6	ASD_DIS	W		**automatic sync detection disable:** Digital Separated Syncs > Digital Composite Sync > Sync On Green
			0*	enable
			1	disable
5	SOGF	W		**sync on green forced:** when set, forces the use of SOGx (where x corresponds to the selected analog video input) input when the automatic sync detection is disabled
			0*	enable
			1	disable
4	DCSF	W		**digital composite sync forced:** when set, forces the use of HCSYNCx (where x corresponds to the selected analog video input) input when the automatic sync detection is disabled
			0*	enable
			1	disable
3 to 0	x	W	0000*	for test: must be set to default value for proper operation

Table 8. SDRS_FLAGS register (address 0Dh) bit description[1]

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	ASD	R		**additional sync pulses detected:** additional sync pulses on the selected analog input
			0*	are not detected
			1	are detected

© NXP B.V. 2008. All rights reserved.

Table 8. SDRS_FLAGS register (address 0Dh) bit description[1] *…continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
6	SOGD2	R		**sync on green detected:** on pin SOG2
			0*	pulses are not detected
			1	pulses are detected
5	-			not used
4	DSSD2	R		**digital separated syncs detected:** on pins VSYNC2 and HCSYNC2
			0*	pulses are not detected
			1	pulses are detected
3	-			not used
2	SOGD1	R		**sync on green detected:** on pin SOG1
			0*	pulses are not detected
			1	pulses are detected
1	-			not used
0	DSSD1	R		**digital separated syncs detected:** on pins VSYNC1 and HCSYNC1
			0*	pulses are not detected
			1	pulses are detected

[1] When one of these bits changes, the VAI_N pin is pulled down until SDRS_FLAGS0 is read.

9.2.4 PLL registers

Table 9. PLL_CTRL register (address 10h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7		R		reserved for test
6 to 4	-	R	-	not used
3	EDG	R		**edge:** synchronizes the PLL on the internal HSYNC pulses
			0*	on the rising edge
			1	on the falling edge
2 to 0		R		reserved for test

[1] By default, the SDRS toggles automatically the HSYNC to have an internal positive HSYNC signal

© NXP B.V. 2008. All rights reserved.

Table 10. PLL_MNDIV registers (address 11h and 12h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
11h	PLL_MNDIV_MSB	7 to 6	MDIV[1:0]	W		**master divider:** selects the master divider to adjust the sampling frequency range with the PLL frequency range from 110 MHz to 200 MHz
					00	divided by 1; > 110 Msample/s
					01	divided by 2; 50 Msample/s to 110 Msample/s
					10	divided by 4; 25 Msample/s to < 50 Msample/s
					11*	divided by 8; 12.5 Msample/s to < 25 Msample/s
		5 to 4	-	W	00*	not used
		3 to 0	NDIV[11:8]	W	3h*	**pixel divider:** pixel division value
12h	PLL_NDIV_LSB	7 to 0	NDIV[7:0]	W	60h*	

Table 11. LOCKFLAG register (address 13h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 2	-	W	00 0000*	not used
1	x	W	0*	for test; must be set to default value for proper operation
0	PLL_LOCK	R		**PLL_lock:** indicates when the PLL is locked
			0*	not locked
			1	locked

9.2.5 Pixel clocks generation registers

Table 12. DLL_PHASE register (address 14h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 5	-	W	000*	not used
4 to 0	PHASE[4:0]	W	1 0000*	**phase:** these bits set the phase shift for the three clock signals CLKPIX, CLKFOR and CLKOUT; it is the fine adjustment of the phase, see Table 15

© NXP B.V. 2008. All rights reserved.

Table 13. PIXCLKGEN_PRST register (address 15h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 5	CLKOUT_PRST[2:0]	W	110*	**output clock preset:** these bits set the phase shift for the output clock CLKOUT; it is the rough adjustment of the phase and there is the same number of steps as the division factor selected for CLKOUT
4 to 3	CLKFOR_PRST[1:0]	W	10*	**formatter clock preset** used to program the phase shift for the 4 : 2 : 2 formatter clock CLKFOR It Is the rough adjustment of the phase and there is the same number of steps than the division factor selected for CLKFOR
2 to 0	CLKPIX_PRST[2:0]	W	111*	**pixel clock preset:** these bits set the phase shift for the ADC and VHREF pixel clock CLKPIX; it is the rough adjustment of the phase and there is the same number of steps as the division factor selected for CLKPIX

Table 14. PIXCLKGEN_CTRL0 register (address 16h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 6	CLKOUT_DIV[1:0]	W		**output clock division factor:** selects the PLL frequency division factor for the output clock CLKOUT. For 4 : 2 : 2 semi-planar or 4 : 4 : 4 output formats, the division factor must be the same as the master division factor. In case of the 4 : 2 : 2 ITU-R BT.656 formats, it must be half of the master division factor
			00*	divide by 2
			01	divide by 4
			10	divide by 8
			11	not defined
5 to 4	CLKFOR_DIV[1:0]	W		**formatter clock division factor:** selects the PLL frequency division factor for the ITU-R BT.656 formatter clock CLKFOR The division factor must be the half of the master division factor
			00	divide by 2
			01	divide by 4
			10	not defined
			11*	not defined
3 to 2	CLKPIX_DIV[1:0]	W		**pixel clock division factor:** selects the PLL frequency division factor for the pixel clock CLKPIX. The division factor must be the same as the master division factor
			00	divide by 2
			01	divide by 4
			10*	divide by 8
			11	not defined

© NXP B.V. 2008. All rights reserved.

Table 14. PIXCLKGEN_CTRL0 register (address 16h) bit description *…continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
1	PR_DEL	W		**phase delay:** delays the rough adjustment of the three clock signals, see Table 15
			0	no delay
			1*	delay of one PLL period
0	PH_CORR	W		**phase correction:** selects the falling or rising edge of the horizontal reference signal from the PLL to synchronize the three clock divisions, see Table 15
			0	falling edge selected
			1*	rising edge selected

Table 15. Relationship between bits PR_DEL, PH_CORR and phase value

PHASE[4:0]	PR_DEL	PH_CORR
0 to 7	0	0
8 to 15	1	1
16 to 31	1	0

Table 16. Relation between master division and clock division

MDIV[1:0]	Master division	4 : 4 : 4 or semi-planar		4 : 2 : 2 ITU-R BT.656		formatter clock		pixel clock	
		CLKOUT_DIV	CLKOUT_PRST	CLKOUT_DIV	CLKOUT_PRST	CLKFOR_DIV	CLKFOR_PRST	CLKPIX_DIV	CLKPIX_PRST
11	8	10	0 to 7	01	0, 1, 2, 3	01	0, 1, 2, 3	10	0 to 7
10	4	01	0 to 3	00	0 or 1	00	0 or 1	01	0 to 3
01	2	00	0 or 1	11	0	11	0	00	0 or 1
00	1	11	0	not available		not available		00	0

9.2.6 Pixel clocks generation registers

Table 17. PIXCLKGEN_CTRL1 register (address 17h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	CLKOUT_TOG	W		**output clock toggle**
			0*	does not toggle the signal CLKOUT
			1	toggles the signal CLKOUT
6 to 4	CLKOUT_SEL[2:0]	W		**output clock selection:** select the clock available on pin VCLK
			000	reserved for test
			001	reserved for test
			010	not defined
			011	not defined
			100*	CLKOUT
			101	CLKFOR
			110	CLKPIX
			111	not defined

© NXP B.V. 2008. All rights reserved.

Table 17. PIXCLKGEN_CTRL1 register (address 17h) bit description *…continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
3 to 2	CLKFOR_SEL[1:0]	W		**formatter clock selection:** select the clock for the ITU-R656 formatter
			00	reserved for test
			01*	CLKFOR
			10	not defined
			11	0
1 to 0	x	W	10*	for test: must be set to default value for proper operation

9.2.7 Clamp levels registers

Table 18. Bright levels registers (address 1Ah to 1Ch) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
1Ah	BRIGHT_GY	7 to 0	BRIGHT_ GY[7:0]	W	10h*	**G/Y brightness:** these bits control the clamp level of the G/Y channel
1Bh	BRIGHT_BU	7 to 0	BRIGHT_ BU[7:0]	W	80h*	**B/P_B brightness:** these bits control the clamp level of the B/P_B channel
1Ch	BRIGHT_RV	7 to 0	BRIGHT_ RV[7:0]	W	80h*	**R/P_R brightness:** these bits control the clamp level of the R/P_R channel

Table 19. Relationship between the brightness code and the clamp level

Programmed code (8-bits)		Clamp code (decimal)
Decimal	Binary MSB/LSB	
0	0000 0000	0
:	:	:
247	1111 0111	247

9.2.8 Video gain registers (GAIN_RV, GAIN_BU, GAIN_GY)

Table 20. R/V video gain registers (addresses 20h to 23h) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
20h	COARSE_GAINRV	7 to 4	-	W		not used
		3 to 0	COARSE_RV[3:0]	W	04h*	**coarse_rv:** coarse gain value for channel R/V
21h	FINE_GAINRV	7	-	W		not used
		6 to 0	FINE_RV[6:0]	W	5Ch*	**fine_rv:** fine gain value for channel R/V
22h	AGC_HIGHRV	7 to 0	HIGH_RV[7:0]	W	F0h*	**high_rv:** AGC high value for channel R/V
23h	AGC_LOWRV	7	-	W		not used
		6 to 0	LOW_RV[6:0]	W	90h*	**low_rv:** AGC low value for channel R/V

© NXP B.V. 2008. All rights reserved.

Table 21. B/U video gain registers (addresses 2Ah to 2Dh) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
2Ah	COARSE_GAINBU	7 to 4	-	W		not used
		3 to 0	COARSE_GY[3:0]	W	04h*	**coarse_bu:** coarse gain value for channel B/U
2Bh	FINE_GAINBU	7	-	W		not used
		6 to 0	FINE_BU[6:0]	W	5Ch*	**fine_bu:** fine gain value for channel B/U
2Ch	AGC_HIGHBU	7 to 0	HIGH_BU[7:0]	W	F0h*	**high_bu:** AGC high value for channel B/U
2Dh	AGC_LOWBU	7	-	W		not used
		6 to 0	LOW_BU[6:0]	W	90h*	**low_bu:** AGC low value for channel B/U

Table 22. G/Y video gain registers (addresses 34h to 37h) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
34h	COARSE_GAINGY	7 to 4	-	W		not used
		3 to 0	COARSE_GY[3:0]	W	04h*	**coarse_gy:** coarse gain value for the channel G/Y
35h	FINE_GAINGY	7	-	W		not used
		6 to 0	FINE_GY[6:0]	W	5Ch*	**fine_gy:** fine gain value for the channel G/Y
36h	AGC_HIGHGY	7 to 0	HIGH_GY[7:0]	W	F0h*	**high_gy:** AGC high value for the channel G/Y
37h	AGC_LOWGY	7	-	W		not used
		6 to 0	LOW_GY[6:0]	W	90h*	**low_gy:** AGC low value for the channel G/Y

9.2.9 Sync timing measurement registers

Table 23. Sync timing measurement registers (address 40h to 44h) bit description

Addr	Register	Bit	Symbol	Access	Value	Description
40h	V_PER_MSB	7 to 0	V_PER[19:12]	R	00h*	**vertical period:** indicates the period of two fields (interlaced) or frames (progressive), counted in MCLK clock periods[1]
41h	V_PER_ISB	7 to 0	V_PER[11:4]	R	00h*	
44h	STM_LSB	7 to 4	V_PER[3:0]	R	0000*	
42h	H_PER_MSB	7 to 0	H_PER[9:2]	R	00h*	**horizontal period:** indicates the period of the line, counted in MCLK clock periods[1]
44h	STM_LSB	3 to 2	H_PER[1:0]	R	00*	
43h	HS_WIDTH_MSB	7 to 0	HS_WIDTH[9:2]	R	00h*	**horizontal sync width:** indicates the width of the horizontal sync pulse, counted in MCLK clock periods[1]
44h	STM_LSB	1 to 0	HS_WIDTH[1:0]	R	00*	

[1] The recommended frequency for MCLK signal is 13.5 MHz.

© NXP B.V. 2008. All rights reserved.

9.2.10 Color space conversion registers

Table 24. MAT_CTRL register (address 80h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 2	-	W	00 0000*	not used
1 and 0	MAT_SC[1:0]	W		**scale factor selection:** fix the scale factor to convert the floating matrix [C_{xy}] into an integer matrix $[P_{xy}]: \begin{bmatrix} P_{11} & P_{12} & P_{13} \\ P_{21} & P_{22} & P_{23} \\ P_{31} & P_{32} & P_{33} \end{bmatrix} = INT\left(S \times \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \right).$ The choice depends on the biggest coefficient in absolute value $\lvert C_{xy} \rvert$:
			00	when $2 \leq \lvert C_{xy} \rvert < 4$; S = 256
			01	when $1 \leq \lvert C_{xy} \rvert < 2$; S = 512
			10*	when $\lvert C_{xy} \rvert < 1$; S = 1024
			11	undefined

Table 25. Offset input registers (address 81h to 86h) bit description

*Legend: * = default value*[1]

Addr	Register	Bit	Symbol	Access	Value	Description
81h	MAT_OI1_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	MAT_OI1[8:6]	W	000*	**offset in 1** compensate the brightness value for the channel G/Y, e.g. with YC_BC_R input, –16 for Y so OFFSET_IN1 = 1111 0000b = F0h[2]
82h	MAT_OI1_LSB	7 to 2	OFFSET_IN1[5:0]	W	00h*	
		1 to 0	-	W	00*	not used
83h	MAT_OI2_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	MAT_OI2[8:6]	W	000*	**offset in 2** compensate the brightness value for the channel R/V, e.g. with YC_BC_R input, –128 for C_R so OFFSET_IN2 = 1000 0000b = 80h[2]
84h	MAT_OI2_LSB	7 to 2	OFFSET_IN2[5:0]	W	00h*	
		1 to 0	-	W	00*	not used

© NXP B.V. 2008. All rights reserved.

Table 25. Offset input registers (address 81h to 86h) bit description *…continued*

*Legend: * = default value*[1]

Addr	Register	Bit	Symbol	Access	Value	Description
85h	MAT_OI3_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	MAT_OI3[8:6]	W	000*	**offset_in3** compensate the brightness value for the channel B/U, e.g. with YC_BC_R input, –128 for C_B so OFFSET_IN3 = 1000 0000b = 80h[2]
86h	MAT_OI3_LSB	7 to 0	OFFSET_IN3[5:0]	W	00h*	
	-	1 to 0	-	W	00*	not used

[1] The default values correspond with the RGB full-scale to YC_BC_R ITU-R BT.601 reduced-scale conversion.

[2] The value is signed 11-bit two's complement integer.

Table 26. Coefficient registers (address 87h to 98h) bit description

*Legend: * = default value*[1]

Addr	Register	Bit	Symbol	Access	Value	Description
87h	MAT_P11_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P11[10:8]	W	010*	**coefficient (1,1):** coefficient from the G/Y channel to the G/Y channel[2]
88h	MAT_P11_LSB	7 to 0	P11[7:0]	W	02h*	
89h	MAT_P12_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P12[10:8]	W	001*	**coefficient (1,2):** coefficient from the R/C_R channel to the G/Y channel[2]
8Ah	MAT_P12_LSB	7 to 0	P12[7:0]	W	06h*	
8Bh	MAT_P13_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P13[10:8]	W	000*	**coefficient (1,3):** coefficient from the B/C_B channel to the G/Y channel[2]
8Ch	MAT_P13_LSB	7 to 0	P13[7:0]	W	64h*	
8Dh	MAT_P21_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P21[10:8]	W	110*	**coefficient (2,1):** coefficient from the G/Y channel to the R/C_R channel[2]
8Eh	MAT_P21_LSB	7 to 0	P21[7:0]	W	89h*	
8Fh	MAT_P22_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P22[10:8]	W	001*	**coefficient (2,2):** coefficient from the R/C_R channel to the R/C_R channel[2]
90h	MAT_P22_LSB	7 to 0	P22[7:0]	W	C0h*	
91h	MAT_P23_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P23[10:8]	W	111*	**coefficient (2,3):** coefficient from the B/C_B channel to the R/C_R channel[2]
92h	MAT_P23_LSB	7 to 0	P23[7:0]	W	B7h*	
93h	MAT_P31_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P31[10:8]	W	110	**coefficient (3,1):** coefficient from the G/Y channel to the B/C_B channel[2]
94h	MAT_P31_LSB	7 to 0	P31[7:0]	W	D7h*	
95h	MAT_P32_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P32[10:8]	W	111*	**coefficient (3,2):** coefficient from the R/C_R channel to the B/C_B channel[2]
96h	MAT_P32_LSB	7 to 0	P32[7:0]	W	69h*	
97h	MAT_P33_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P33[10:8]	W	001*	**coefficient (3,3):** coefficient from the B/C_B channel to the B/C_B channel[2]
98h	MAT_P33_LSB	7 to 0	P33[7:0]	W	C0h*	

[1] The default values of the coefficients correspond with the RGB full-scale to YC_BC_R ITU-R BT601 reduced scale conversion.

[2] The value is signed 11-bit two's complement integer.

© NXP B.V. 2008. All rights reserved.

Table 27. Offset output registers (address 99h to 9Eh) bit description

*Legend: * = default value*[1]

Addr	Register	Bit	Symbol	Access	Value	Description
99h	MAT_OO1_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	OFFSET_OUT1[10:8]	W	000*	**offset output 1:** the new brightness values for the channel G/Y, e.g. with YC_BC_R output, 16 for Y so OFFSET_OUT1 = 0 0001 0000b = 10h[2]
9Ah	MAT_OO1_LSB	7 to 0	OFFSET_OUT1[7:0]	W	40h*	
9Bh	MAT_OO2_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	OFFSET_OUT2[10:8]	W	010*	**offset output 2:** the new brightness values for the channel R/V e.g. with YC_BC_R output, 128 for C_R so OFFSET_OUT2 = 0 1000 0000b = 80h[2]
9Ch	MAT_OO2_LSB	7 to 0	OFFSET_OUT2[7:0]	W	00h*	
9Dh	MAT_OO3_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	OFFSET_OUT3[10:8]	W	010*	**offset output 3:** the new brightness values for the channel B/U e.g. with YC_BC_R output, 128 for C_B so OFFSET_OUT3 = 0 1000 0000b = 80h[2]
9Eh	MAT_OO3_LSB	7 to 0	OFFSET_OUT3[7:0]	W	00h*	
9Fh	MAT_BYPASS	7 to 1	-	W	00h*	not used
		0	MAT_BP	W		**matrix bypassed:** bypasses or not the matrix and offsets conversion
					0	not bypassed
					1*	bypassed

[1] The default values correspond with the RGB full-scale to YC_BC_R ITU-R BT.601 reduced-scale conversion.

[2] The value is signed 11-bit two's complement integer.

9.2.11 Line and pixel counters

Table 28. Pixel counter registers (address A1h to A3h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
A1h	PXCNT_PR_LSB	7 to 0	PXCNT_PR[7:0]	W	03h*	**pixel counter preset:** preset value stored in the pixel counter on the rising edge of the internal HSYNC
A2h	PXCNT_MSB	7 to 4	PXCNT_PR[11:8]	W	0h*	
		3 to 0	PXCNT_NPIX[11:8]	W	3h*	**pixel counter number of pixels:** modulo of the pixel counter; this counter counts from 1 to PXCNT_NPIX and rolls-over to 1; the recommended value is the total number of pixels per line
A3h	PXCNT_NPIX_LSB	7 to 0	PXCNT_NPIX[7:0]	W	60h*	

Table 29. Line counter registers (address A4h to A6h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
A4h	LCNT_PR_LSB	7 to 0	LCNT_PR[7:0]	W	01h*	**line counter preset:** preset value stored in the line counter on the rising edge of the internal VSYNC
A5h	LCNT_MSB	7 to 4	LCNT_PR[11:8]	W	0h*	
		3 to 0	LCNT_NLIN[11:8]	W	0h*	**line counter number of lines:** modulo of the line counter; this counter counts from 1 to LCNT_NLIN and rolls-over to 1; the recommended value is the total number of lines per frame; if value is set to 000h the line counter uses the value of MEAS_LINES
A6h	LCNT_NLIN_LSB	7 to 0	LCNT_NLIN[7:0]	W	00h*	

© NXP B.V. 2008. All rights reserved.

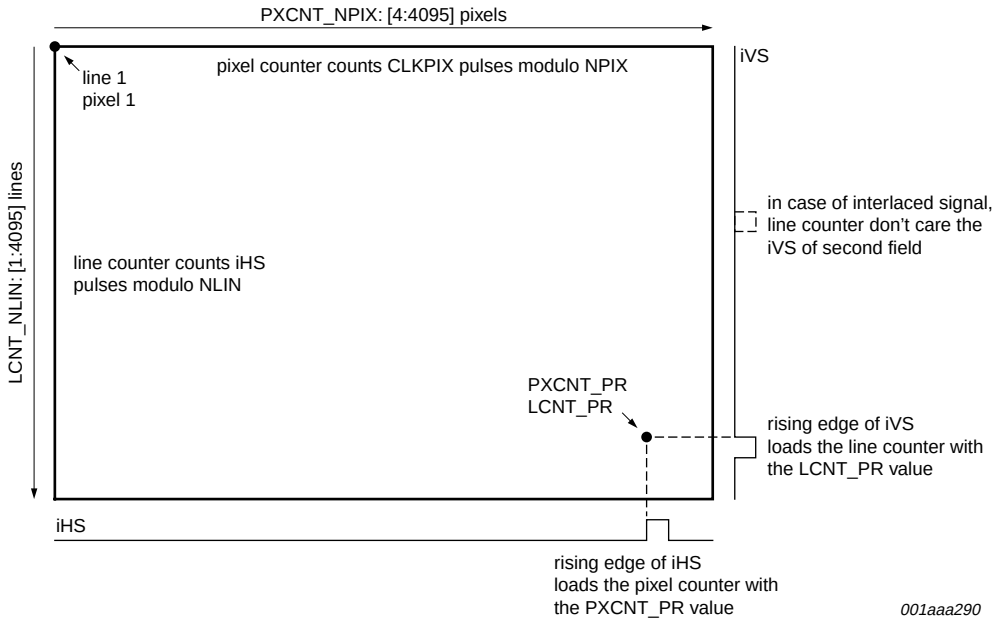


Fig 4. Line and pixel counters

Table 30. Horizontal reference registers (address A7h to A9h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
A7h	HREF_S_LSB	7 to 0	HREF_START[7:0]	W	00h*	**horizontal reference start:** index of the first active pixel, and also the position of the rising edge of HREF signal and the position of SAV; if null, HREF stays LOW and no SAV is inserted in the data stream
A8h	HREF_MSB	7 to 4	HREF_START[11:8]	W	0h*	
		3 to 0	HREF_END[11:8]	W	0h*	**horizontal reference end (LSB):** index after the last active pixel, and also the position of the falling edge of HREF signal and the position of EAV; if null, HREF falls at the beginning of a new line and no EAV is inserted in the data stream
A9h	HREF_E_LSB	7 to 0	HREF_END[7:0]	W	00h*	

Table 31. Horizontal reference registers (address AAh to ACh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
AAh	HS_S_LSB	7 to 0	HS_START[7:0]	W	00h*	**horizontal sync start:** define the position of the rising edge of the HS signal generated by the timing generator[1]
ABh	HS_MSB	7 to 4	HS_START[11:8]	W	0h*	
		3 to 0	HS_END[11:8]	W	0h*	**horizontal sync end:** define the position of the falling edge of the HS signal generated by the timing generator[1]
ACh	HS_E_LSB	7 to 0	HS_END[7:0]	W	00h*	

[1] If 0, HS signal corresponds with the horizontal sync internal signal.

© NXP B.V. 2008. All rights reserved.

Table 32. Vertical reference registers (address ADh to B2h) bit description[1]

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
ADh	VREF_F1_S_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	VREF_F1_START[10:8]	W	000*	**vertical reference start for field 1:** index of the first blanking line for field 1, and also the position of the rising edge of VREF signal and the value of bit V in SAV/EAV code; if 0, VREF stays LOW
AEh	VREF_F1_S_LSB	7 to 0	VREF_F1_START[7:0]	W	00h*	
AFh	VREF_F1_WIDTH	7 to 0	VREF_F1_WIDTH[7:0]	W	00h*	**vertical reference width for field 1:** width of the vertical blanking for field 1, and also the width of VREF signal and the value of bit V in SAV/EAV code; if 0, VREF stays LOW
B0h	VREF_F2_S_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	VREF_F2_START[10:8]	W	000*	**vertical reference start for field 2:** index of the first blanking line for field 2, and also the position of the rising edge of VREF signal and the value of bit V in SAV/EAV code
B1h	VREF_F2_S_LSB	7 to 0	VREF_F2_START[7:0]	W	00h*	
B2h	VREF_F2_WIDTH	7 to 0	VREF_F2_WIDTH[7:0]	W	00h*	**vertical reference width for field 2:** width of the vertical blanking for field 2, and also the width of VREF signal and the value of bit V in SAV/EAV code

[1] In progressive case, bits VREF_F2_START[10:0] and VREF_F2_WIDTH[7:0] must be set to logic 0.

Table 33. Vertical sync registers (address B3h to BEh) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
B3h	VS_F1_LINE_S_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	VS_F1_LINE_START[10:8]	W	000*	**vertical sync line start for field 1:** position in number of lines of the VS signal generated by the timing generator for the field 1; if 0, VS stays LOW
B4h	VS_F1_LINE_S_LSB	7 to 0	VS_F1_LINE_START[7:0]	W	00h*	
B5h	VS_F1_LINE_WIDTH	7 to 0	VS_F1_LINE_WIDTH[7:0]	W	00h*	**vertical sync line width for field 1:** width in number of lines of the VS signal generated by the timing generator for field 1; if 0, VS stays LOW
B6h	VS_F2_LINE_S_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	VS_F2_LINE_START[10:8]	W	000*	**vertical sync line start for field 2:** position in number of lines of the VS signal generated by the timing generator for the field 2[1]
B7h	VS_F2_LINE_S_LSB	7 to 0	VS_F2_LINE_START[7:0]	W	00h*	
B8h	VS_F2_LINE_WIDTH	7 to 0	VS_F2_LINE_WIDTH[7:0]	W	00h*	**vertical sync line width for field 2:** width in number of lines of the VS signal generated by the timing generator for field 2[1]

© NXP B.V. 2008. All rights reserved.

Table 33. Vertical sync registers (address B3h to BEh) bit description *…continued*

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
B9h	VS_F1_PIX_S_LSB	7 to 0	VS_F1_PIX_START[7:0]	W	01h*	**vertical sync pixel start for field 1:** position in number of pixels of the rising edge of the VS signal generated by the timing generator for field 1; if 0, VS stays LOW
BAh	VS_F1_PIX_MSB	7 to 4	VS_F1_PIX_START[11:8]	W	0h*	
		3 to 0	VS_F1_PIX_END[11:8]	W	0h*	**vertical sync pixel end for field 1 (LSB):** position in number of pixels of the falling edge of the VS signal generated by the timing generator for field 1; if 0, VS stays LOW
BBh	VS_F1_PIX_E_LSB	7 to 0	VS_F1_PIX_END[7:0]	W	01h*	
BCh	VS_F2_PIX_S_LSB	7 to 0	VS_F2_PIX_START[7:0]	W	01h*	**vertical sync pixel start for field 2:** position in number of pixels of the rising edge of the VS signal generated by the timing generator for field 2
BDh	VS_F2_PIX_MSB	7 to 4	VS_F2_PIX_START[11:8]	W	0h*	
		3 to 0	VS_F2_PIX_END[11:8]	W	0h*	**vertical sync pixel end for field 2:** position in number of pixels of the falling edge of the VS signal generated by the timing generator for field 2
BEh	VS_F2_PIX_E_LSB	7 to 0	VS_F2_PIX_END[7:0]	W	01h*	

[1] In progressive case bits VS_F2_LINE_START[12:0] and VS_F2_LINE_WIDTH[7:0] must be set to logic 0.

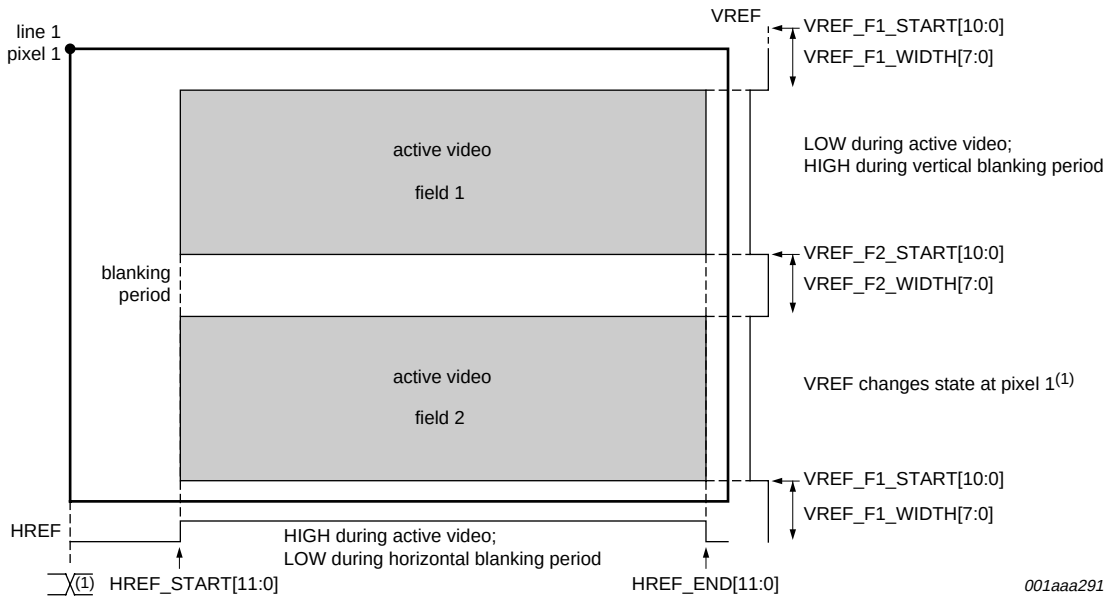


Fig 5. HREF and VREF in interlaced case

© NXP B.V. 2008. All rights reserved.

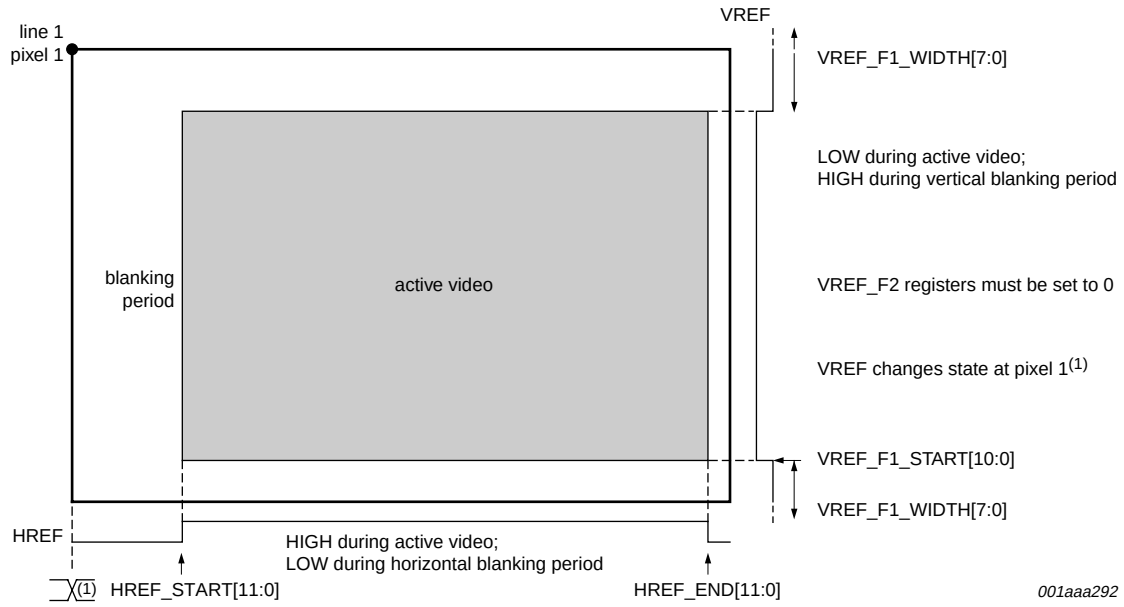


Fig 6. HREF and VREF in progressive case

Table 34. Field reference registers (address BFh to C1h) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
BFh	FREF_F1_S_LSB	7 to 0	FREF_F1_START[7:0]	W	00h*	**field reference for field 1 start (LSB):** index of the first line for field 1 which corresponds to the line where the FREF signal toggles, see register FREF_POL_MSB bit 6 to bit 4
C0h	FREF_POL_MSB	7	FPOL	W		**field polarity:** defines the polarity of the FREF signal and bit F in the SAV/EAV code
					0*	field 1 is LOW and field 2 is HIGH
					1	field 1 is HIGH and field 2 is LOW
		6 to 4	FREF_F1_START[10:8]	W	000*	**field reference for field 1 start (MSB):** index of the first line for field 1 which corresponds to the line where the FREF signal toggles, see register FREF_F1_S_LSB bit 7 to bit 0
		3	-	W	0*	not used
		2 to 0	FREF_F2_START[10:8]	W	000*	**field reference for field 2 start:** index of the first line for field 2 which corresponds to the line where the FREF signal toggles
C1h	FREF_F2_S_LSB	7 to 0	FREF_F2_START[7:0]	W	00h*	

© NXP B.V. 2008. All rights reserved.

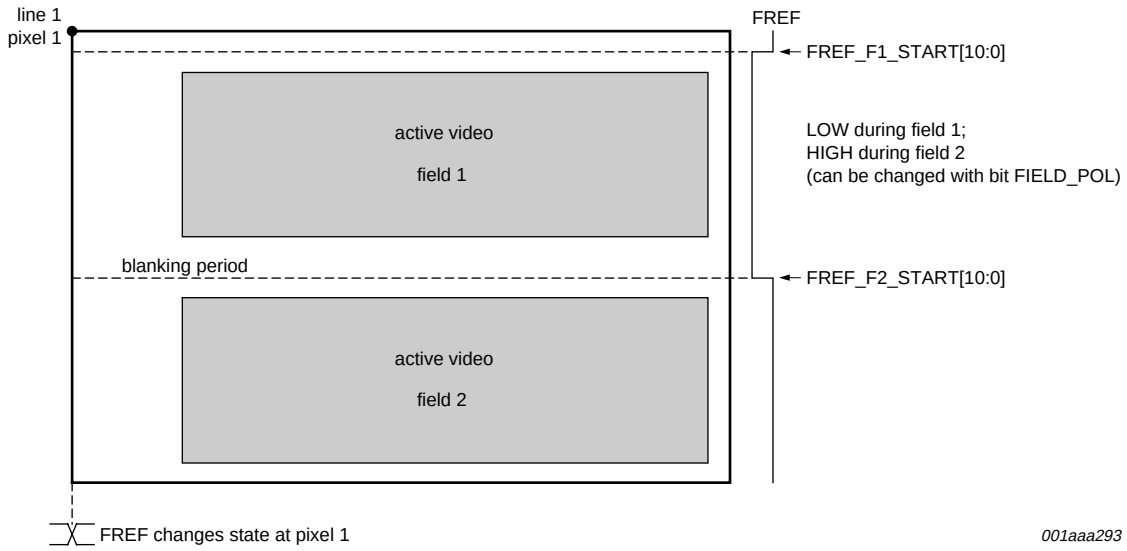


Fig 7. FREF in interlaced case

Table 35. Clamp signal registers (address C8h to CAh) bit description[1]

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
C8h	CLAMP_PIX_S_LSB	7 to 0	CLAMP_ PIX_ START[7:0]	W	00h*	**clamp signal pixel start:** position, in number of pixels, of the beginning of the clamp signal generated by the timing generator
C9h	CLAMP_PIX_MSB	7 to 4	CLAMP_ PIX_ START[11:8]	W	0h*	
		3 to 0	CLAMP_ PIX_ END[11:8]	W	0h*	**clamp signal pixel end:** position, in number of pixels, of the end of the clamp signal generated by the timing generator
CAh	CLAMP_PIX_E_LSB	7 to 0	CLAMP_PIX_ END[7:0]	W	00h*	

[1] Minimum width of the clamp pulse is 40 pixels and it must be active only during the horizontal back porch.

Table 36. CLP_Fx_LINE_nnn registers (address CBh to D0h) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
CBh	CLP_F1_LINE_S_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	CLAMP_F1_ LINE_ START[10:8]	W	000*	**clamp signal line start for field 1 (LSB):** position, in number of lines, from which no clamp pulses are generated for field 1, typically during the vertical pulse in case of the sync on green signal
CCh	CLP_F1_LINE_S_LSB	7 to 0	CLAMP_F1_LINE_START[7:0]	W	00h*	
CDh	CLP_F1_LINE_WIDTH	7 to 0	CLAMP_F1_LINE_WIDTH[7:0]	W	00h*	**clamp signal line width for field 1:** width, in number of lines, where no clamp pulses are generated for field 1

© NXP B.V. 2008. All rights reserved.

Table 36. CLP_Fx_LINE_nnn registers (address CBh to D0h) bit description *...continued*

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
CEh	CLP_F2_LINE_S_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	CLAMP_F2_LINE_START[10:8]	W	000*	**clamp signal line start for field 2 (LSB):** position, in number of lines, from which no clamp pulses are generated for field 2, typically during the vertical pulse in case of the sync on green signal
CFh	CLP_F2_LINE_S_LSB	7 to 0	CLAMP_F2_LINE_START[7:0]	W	00h*	
D0h	CLP_F2_LINE_WIDTH	7 to 0	CLAMP_F2_LINE_WIDTH[7:0]	W	00h*	**clamp signal line width for field 2:** width, in number of lines, where no clamp pulses are generated for field 2

Table 37. GAIN signal registers (address D1h to D3h) bit description[1]

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
D1h	GAIN_S_LSB	7 to 0	GAIN_START[7:0]	W	00h*	**gain start signal:** position of the gain signal generated by the timing generator
D2h	GAIN_MSB	7 to 4	GAIN_ START[11:8]	W	0h*	
		3 to 0	GAIN_ END[11:8]	W	0h*	**gain end signal:** position of the end of the gain signal generated by the timing generator
D3h	GAIN_E_LSB	7 to 0	GAIN_END[7:0]	W	51h*	

[1] The minimum width of the gain pulse (GAIN_END – GAIN_START) is 80 pixels and can include the horizontal sync pulse. The gain pulse and the clamp pulse should not overlap.

Table 38. Horizontal sync registers (address D4h to D6h) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
D4h	FDW_S_LSB	7 to 0	FDW_START[7:0]	W	00h*	**frame detection window start:** position of the start of the frame detection window; the recommended value is $^{7}/_{8}$ of total number of pixels per line
D5h	FDW_MSB	7 to 4	FDW_START[11:8]	W	0h*	
		3 to 0	FDW_END[11:8]	W	0h*	**frame detection window end:** position of the end of the frame detection window; the recommended value is $^{3}/_{8}$ of total number of pixels per line
D6h	FDW_E_LSB	7 to 0	FDW_END[7:0]	W	00h*	

© NXP B.V. 2008. All rights reserved.

Table 39. Measured lines and pixels registers (address D7h to DAh) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
D7h	ASD_MEASLIN_MSB	7	INTD	R		**interlaced detected:** indicates an interlaced or progressive signal
					0*	progressive
					1	interlaced
		6	AUTO_OK	R		**automatic detection:** the number of measured lines per frame
					0*	correspond to 625 or 525 (±2 lines of tolerance)
					1	the timing generator is forced to 576i or 480i standard
		5	525	R		**interlaced detected:** when AUTO_OK = 1
					0*	is forced to 480i standard
					1	525 (±2 lines of tolerance) lines per frame are counted
		4 to 3	-	R		not used
		2 to 0	MEAS_LINES[10:8]	R	000*	**measured number of lines:** indicates the number of lines per frame measured by the timing generator
D8h	MEASLIN_LSB	7 to 0	MEAS_LINES[7:0]	R	00h*	
D9h	MEASPIX_MSB	7 to 4	-	R	0h*	not used
		3 to 0	MEAS_PIX[11:8]	R	0h*	**measured number of pixels:** indicates the number of pixels per line measured by the timing generator; in Analog mode, the value is the same as the PLL division value
DAh	MEASPIX_LSB	7 to 0	MEAS_PIX[7:0]	R	00h*	

Table 40. Blanking code registers (address DCh to DFh) bit description[1]

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
DCh	BLK_GY_LSB	7 to 2	BLK_GY[5:0]	W	10h*	blanking code of the G/Y channel (MSB), see address DFh bit 7 to bit 6
		1 to 0	-	W		not used
DDh	BLK_BU_LSB	7 to 2	BLK_BU[5:0]	W	80h*	blanking code of the B/C_B channel (MSB), see address DFh bit 4 to bit 3
		1 to 0	-	W		not used
DEh	BLK_RV_LSB	7 to 2	BLK_RV[5:0]	W	80h*	blanking code of the R/C_R channel (MSB), see address DFh bit 1 to bit 0
		1 to 0	-	W		not used
DFh	BLK_MSB	7 to 6	BLK_GY[7:6]	W	00*	blanking code bits 7 and 6 of the G/Y channel (MSB), see address DCh
		5	-	W	0*	not used
		4 to 3	BLK_BU[7:6]	W	10*	blanking code bits 7 and 6 of the B/C_B channel (MSB), see address DDh
		2	-	W	0*	not used
		1 to 0	BLK_RV[7:6]	W	10*	blanking code bits 7 and 6 of the R/C_R channel (MSB), see address DEh

© NXP B.V. 2008. All rights reserved.

[1] These register control the blanking code of the x/x channel; this code is output during the horizontal blanking (HREF is LOW) or the vertical blanking (VREF is HIGH)

9.2.12 Prefiltering register (PRE_FILTERS)

This register is used to downsample the R/P_R and B/P_B channels for the YUV 4 : 2 : 2 semi-planar and ITU-R BT.656 formats.

Table 41. PRE_FILTER register (address E0h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 and 6	-	W	00*	not used
5 and 4	FILTER_BU[1:0]	W		**B/C_B downsampling filter:** enables the shape of the prefilter for the B/C_B channel
			00	no filter (used in 4 : 4 : 4 mode)
			01	average of two samples
			10*	simple 7-taps filter
			11	27 taps ITU-R BT.601 compliant half-band filter
3 and 2	-	W	00*	not used
1 and 0	FILTER_RV[1:0]	W		**R/C_R downsampling filter:** enables the shape of the prefilter for the R/C_R channel
			00	no filter (used in 4 : 4 : 4 mode)
			01	average of two samples
			10*	simple 7-taps filter
			11	27 taps ITU-R BT.601 compliant half-band filter

9.2.13 Range control registers

Table 42. Range control registers (address E1h to E4h) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
E1h	OF_CCEIL	7 to 6	-	W		not used
		5 to 0	C_CEIL[5:0]	W	C0h*	**chrominance ceiling level:** fix the maximum code of B/C_B and R/C_R channels[1]
E2h	OF_CFLOOR	7 to 6	-	W		not used
		5 to 0	C_FLOOR[5:0]	W	40h*	**chrominance floor level:** fix the minimum code of B/C_B and R/C_R channels[2]
E3h	OF_YCEIL	7 to 6	-	W		not used
		5 to 0	Y_CEIL[5:0]	W	ACh*	**luminance ceiling level:** fix the maximum code of the G/Y channel[1]
E4h	OF_YFLOOR	7 to 6	-	W		not used
		5 to 0	Y_FLOOR[5:0]	W	40h*	**luminance floor level:** fix the minimum code of G/Y channel[2]

[1] The maximum level can be chosen between the code words C0h (00h programmed) and FFh (3Fh programmed), the 2 MSBs are set to logic 1 by the device; all higher codes are truncated.

[2] The minimum level can be chosen between the code words 000h (00h programmed) and 0FFh (FFh programmed), the 2 MSBs are set to logic 0 by the device; all lower codes are truncated.

© NXP B.V. 2008. All rights reserved.

9.2.14 Output formatter register

Table 43. OF_CTRL register (address E5h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	OUT	W		**output control:** sets the outputs (VPA[11:0], VPB[11:0], VPC[11:0], VCLK, HS, VS, CS, HREF, VREF, FREF, DE, OR_R, OR_B, OR_G, CTL0 to CTL3, PL)
			0*	outputs active
			1	outputs high-impedance
6	VPL	W		**video ports LOW**
			0	forces the unused video port outputs to high-impedance
			1*	forces the unused video port outputs to LOW
5	-	W	-	not used
4	BLC	W		**blanking codes**
			0*	inserts the blanking codes
			1	removes the blanking codes
3	TRC	W		**timing reference codes**
			0*	inserts the timing reference codes; the signals HREF and VREF must be programmed into the VHREF timing generator to insert the timing reference codes; timing reference codes are inserted in all video port streams and are present during the vertical blanking; see Table 44
			1	removes the timing reference codes
2	-	W	0*	for test; must be set to logic 0 for proper operation
1 and 0	FOR_SEL[1:0]	W		**formatter selection**
			00	4 : 4 : 4 format[1]
			01	4 : 2 : 2 semi-planar format[2]
			10*	4 : 2 : 2 ITU-R BT.656 format[3]
			11	undefined

[1] In 4 : 4 : 4, the video is output on three video ports, one per color.

[2] In 4 : 2 : 2 semi-planar, the video is output on two video ports, one for luminance (Y) and one for chrominance (C_B and C_R alternately).

[3] In 4 : 2 : 2 ITU-R BT.656, the video is output on one video port (C_B-Y-C_R-Y sequence).

Table 44. Timing reference codes

Codeword	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
3FFh	1	1	1	1	1	1	1	1	1	1
000h	0	0	0	0	0	0	0	0	0	0
000h	0	0	0	0	0	0	0	0	0	0
SAV/EAV[1]	1	F	V	H	P3	P2	P1	P0	0	0

[1] F = 0 during field 1; F = 1 during field 2; V = 1 during field blanking; V = 0 elsewhere; H = 0 in SAV, H = 1 in EAV and P0 to P3 are protection bits.

© NXP B.V. 2008. All rights reserved.

9.2.15 Sync output selection registers

Table 45. CSVSHS_SEL register (address E8h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 5	CS_SEL[2:0]	W		**composite sync selection:** selects the signal outputs on pin CS
			000*	composite signal from the SDRS
			001	combination of HS and VS
			xxx	for test
4 to 3	VS_SEL[1:0]	W		**vertical sync selection:** selects the signal outputs on pin VS
			00*	vertical sync from the SDRS
			01	vertical sync from the VHREF timing generator
			10	undefined
			11	undefined
2 to 0	HS_SEL[2:0]	W		**horizontal sync selection:** selects the signal outputs on HS pin
			000*	horizontal sync from the PLL output
			001	for test
			010	horizontal sync from the SDRS
			011	horizontal sync from the HDMI receiver
			100	HS signal generated by the VHREF timing generator
			101	undefined
			110	undefined
			111	undefined

9.2.16 Output polarity control register

Table 46. POL_CTRL register (address E9h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 6	-	W		not used
5	CS_POL	W		**composite sync polarity:** pin CS; composite sync signal
			0*	does not toggle; positive signal
			1	toggles; negative signal
4	HS_POL	W		**horizontal sync polarity:** pin HS; horizontal sync signal
			0*	does not toggle; positive signal
			1	toggles; negative signal
3	VS_POL	W		**vertical sync polarity:** pin VS; vertical sync signal
			0*	does not toggle; positive signal
			1	toggles; negative signal
2	FREF_POL	W		**field reference polarity:** pin FREF; field reference signal
			0*	does not toggle; positive signal
			1	toggles; negative signal

© NXP B.V. 2008. All rights reserved.

Table 46. POL_CTRL register (address E9h) bit description *...continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
1	HREF_POL	W		**horizontal reference polarity:** pin HREF; horizontal reference signal
			0*	does not toggle; positive signal
			1	toggles; negative signal
0	VREF_POL	W		**vertical reference polarity:** pin VREF; vertical reference signal
			0*	does not toggle; positive signal
			1	toggles; negative signal

9.2.17 Video ports control register

Table 47. OUTPUT_CTRL register (address EAh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 and 6	-	W		not used
5 and 4	VPC_SEL[1:0]	W	10*	**video port C selection:** select the data stream to be output on video port C; see Table 48
3 and 2	VPB_SEL[1:0]	W	01*	**video port B selection:** select the data stream to be output on video port B; see Table 48
1 and 0	VPA_SEL[1:0]	W	00*	**video port A selection:** select the data stream to be output on video port A; see Table 48

Table 48. Data stream selection

VPx_SEL[1:0]	4 : 4 : 4 RGB	4 : 4 : 4 YC_BC_R	4 : 2 : 2 YC_BC_R semi-planar	4 : 2 : 2 YC_BC_R ITU-R BT.656
00	R	V	C_B-C_R	C_B-Y-C_R-Y
01	B	U	not used (VPL)	not used (VPL)
10	G	Y	Y	not used (VPL)
11	high-impedance	high-impedance	high-impedance	high-impedance

9.2.18 Data enable signal control register

Table 49. DE_CTRL register (address EBh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	HR_PXQ	W		**horizontal reference pixel qualification:** HREF signals the XAV-codes
			0*	not signaled
			1	signaled
6	HR_SEL	W		**horizontal reference selection:** HREF dependence of VREF
			0*	independent of VREF
			1	logic combination (HREF AND $\overline{VREF}$)

© NXP B.V. 2008. All rights reserved.

Table 49. DE_CTRL register (address EBh) bit description *…continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
5	DE_PXQ	W		**data enable pixel qualification:** expands or not the data enable signal to include the SAV/EAV codes
			0*	does not expand
			1	expands
4	DE_POL	W		**data enable polarity:** selects the signal outputs on pin DE
			0*	does not toggle
			1*	toggles
3 to 0	-		-	not used

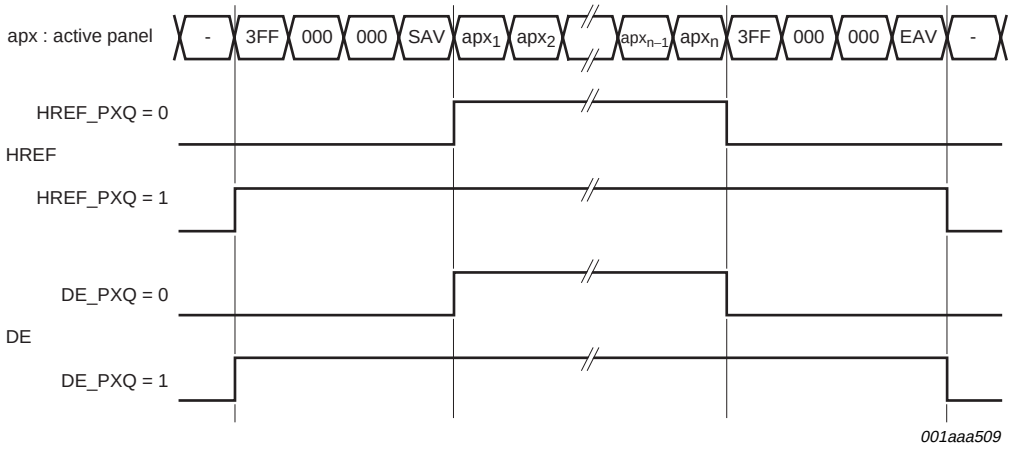


Fig 8. Pixel qualification

9.2.19 Software reset registers

Table 50. RESET_CNTRL register (address F1h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 5	-	W	-	not used
4	RST_MAN	W		**reset manual:** activates the manual software reset for the digital clamp loop, the video gain and the digital processing
			0*	automatic mode; the reset is enabled when no activity is detected
			1	manual mode
3	RST_AVI	W		**software reset analog video interface:** resets the digital clamp loop and the registers depending on the CLKPIX clock in manual mode
			0*	normal operation
			1	reset mode
2 to 0	-	W	-*	not used

© NXP B.V. 2008. All rights reserved.

Registers that are reset to the default value are as follows:

- Video gain registers (address 20h to 3Eh)
- Color space conversion registers (address 80h to 9Eh)
- VHREF timing registers (address A0h to DFh)
- Prefiltering registers (address E0h)
- Output formatter registers (address E1h to E5h)
- Output register (address E9h to EBh)

Register CSVBHS_SEL (address E8h) is not reset.

9.2.20 Power-down control registers

Table 51. PD_AVI_CTRL0 register (address F4h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 5	-	W	0*	not used
4	PD_SOG2	W		**power-down SOG2:** enables the power-down of the slicer of input 2
			0*	normal operation
			1	Power-down mode
3	PD_SOG1	W		**power-down SOG1:** enables the power-down of the slicer of input 1
			0*	normal operation
			1	Power-down mode
2	PD_DLL	W		**power-down DLL:** enables the power-down of the delay-locked loop
			0*	normal operation
			1	Power-down mode
1	PD_PLL	W		**power-down PLL:** enables the power-down of the PLL
			0*	normal operation
			1	Power-down mode
0	PD_AVI	W		**power-down AVI:** enables the power-down of the analog video interface
			0*	normal operation
			1	Power-down mode

Table 52. PD_AVI_CTRL1 register (address F5h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 3	-	W	-	not used
2	PD_ADC_BU	W		**power-down B/P_B ADC:** enables the power-down of the blue channel (B/P_B) ADC
			0*	normal operation
			1	Power-down mode

© NXP B.V. 2008. All rights reserved.

Table 52. PD_AVI_CTRL1 register (address F5h) bit description *...continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
1	PD_ADC_GY	W		**power-down G/Y ADC:** enables the power-down of the green channel (G/Y) ADC
			0*	normal operation
			1	Power-down mode
0	PD_ADC_RV	W		**power-down R/P_R ADC:** enables the power-down of the red channel (R/P_R) ADC
			0*	normal operation
			1	Power-down mode

Table 53. FVH_SEL register (address F6h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 1	-	W	-	not used
0	FVH_SEL	W		**timing signals:** defiines the output on pins 15, 16 and 17
			0	HREF; VREF; FREF
			1*	HS; VS; CS

Table 54. LSB_OUT_SEL register (address F7h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 0	LSB_SEL	W		**LSB signal:** selects the signal on the LSB pin of each digital port (pins 75, 88 and 100).
			00h*	VPA[0]; VPB[0]; VPC[0]
			81h	HREF; VREF; FREF
			82h	ORGY; ORBU; ORRV

Table 55. ORX_SEL register (address F9h) bit description[1][2]

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 and 6	-	W		**Orr signals:** selects the signal applied on internal Orr (over range channel red) signal
			00	**or_rv_agc:** an ADC output underflow or overflow of the range defined by the registers 22h and 23h
			01	**or_rv_datapath:** an ADC output underflow or overflow of the range defined by the registers E1h and E2h
			10	**gain:** monitors the gain calibration signal. see Figure 12 and Figure 13

© NXP B.V. 2008. All rights reserved.

Table 55. ORX_SEL register (address F9h) bit description[1][2] *…continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
5 to 3	-	W		**Org signals:** selects the signal applied on internal Org (over range channel green) signal
			x00	**or_gy_agc:** an ADC output underflow or overflow of the range defined by the registers 36h and 37h
			x01	**or_gy_datapath:** an ADC output underflow or overflow of the range defined by the registers E3h and E4h
			x10	**clamp:** monitors the clamp calibration signal. see Figure 12 and Figure 13
2 to 0	-	W		**Orb signals:** selects the signal applied on internal Orb (over range channel blue) signal
			x00	**or_bu_agc:** an ADC output underflow or overflow of the range defined by the registers 2Ch and 2Dh
			x01	**or_bu_datapath:** an ADC output underflow or overflow of the range defined by the registers E1h and E2h

[1] Defines the internal signals on ORGY, ORBU and ORRV.

[2] The signals are not effected by changing the position of the digital output ports with register EAh.

10. Limiting values

Table 56. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDx(3V3)}$	supply voltage on all 3.3 V pins		–0.5	+4.6	V
$V_{DDx(1V8)}$	supply voltage on all 1.8 V pins		–0.5	+2.5	V
ΔV_{DD}	supply voltage difference		–0.5	+0.5	V
V_I	input voltage		–0.5	V_{DD} + 0.5	V
		5 V tolerant	–0.5	+6.0	V
I_O	output current		-	35	mA
T_{stg}	storage temperature		–40	+125	°C
T_{amb}	ambient temperature		0	70	°C
T_j	junction temperature		-	150	°C
V_{esd}	electrostatic discharge voltage	human body model	2000	-	V

11. Thermal characteristics

Table 57. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	29.7	K/W

© NXP B.V. 2008. All rights reserved.

12. Characteristics

Table 58. Characteristics

$V_{DDA(3V3)}$ = $V_{DDI(3V3)}$ = $V_{DDO(3V3)}$ = 3.15 V to 3.45 V; $V_{DDA(1V8)}$ = $V_{DDC(1V8)}$ = 1.75 V to 1.85 V; T_{amb} = 0 °C to 70 °C; typical values measured at $V_{DDA(3V3)}$ = $V_{DDI(3V3)}$ = $V_{DDO(3V3)}$ = 3.3 V, $V_{DDA(1V8)}$ = $V_{DDC(1V8)}$ = 1.8 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		3.15	3.3	3.45	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		1.75	1.8	1.85	V
$V_{DDI(3V3)}$	input supply voltage (3.3 V)		3.15	3.3	3.45	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		1.75	1.8	1.85	V
$V_{DDO(3V3)}$	output supply voltage (3.3 V)		3.15	3.3	3.45	V
$I_{DDA(1V8)}$	analog supply current (1.8 V)		-	151	160	mA
$I_{DDA(3V3)}$	analog supply current (3.3 V)		-	33	40	mA
$I_{DDI(3V3)}$	input supply current (3.3 V)		-	48	-	mA
$I_{DDO(3V3)}$	output supply current (3.3 V)		-	48	80	mA
$I_{DDC(1V8)}$	core supply current (1.8 V)		-	96	115	mA
$\Delta V_{DD(1V8-1V8)}$	supply voltage difference between two 1.8 V supplies	start-up and established conditions	–0.15	-	+0.15	V
$\Delta V_{DD(3V3-3V3)}$	supply voltage difference between two 3.3 V supplies	start-up and established conditions	–0.3	-	+0.3	V
$\Delta V_{DD(3V3-1V8)}$	supply voltage difference between one 3.3 V supply and one 1.8 V supply	start-up and established conditions	1.35	-	1.65	V
P	power dissipation	analog interface; f_s = 170 MHz	-	750	945	mW
P_{pd}	power dissipation in power-down mode	I^2C-bus and activity detection power-up	-	47	74	mW
Analog inputs (R1, R2, G1, G2, B1, B2)						
B_{-3dB}	–3 dB bandwidth	channel plus multiplexer	350	380	400	MHz
G	gain	minimum gain; code = 0	-	0	-	dB
		maximum gain; code = 4095	-	5	-	dB
$\Delta G/(G \times \Delta T)$	relative gain variation over temperature		-	0.003	0.008	ppm/°C
$V_{i(p-p)}$	peak-to-peak input voltage	black-to-white	0.65	0.7	0.9	V
C_i	input capacitance		-	0.3	-	pF
$M_{G(CTC)(rms)}$	channel-to-channel gain matching (RMS value)		-	2.5	6.7	%
Sync on green/luminance inputs (SOG1, SOG2), see Figure 9						
t_d	delay time	sync pulse	-	108	-	ns
t_r	rise time	10 % to 90 %; bi-level or tri-level horizontal sync pulse; 4 clock interval	-	320	-	ns
t_f	fall time	90 % to 10 %; bi-level or tri-level horizontal sync pulse; 4 clock interval	-	320	-	ns

© NXP B.V. 2008. All rights reserved.

Table 58. Characteristics *...continued*

$V_{DDA(3V3)} = V_{DDI(3V3)} = V_{DDO(3V3)} = 3.15$ V to 3.45 V; $V_{DDA(1V8)} = V_{DDC(1V8)} = 1.75$ V to 1.85 V; $T_{amb} = 0$ °C to 70 °C; typical values measured at $V_{DDA(3V3)} = V_{DDI(3V3)} = V_{DDO(3V3)} = 3.3$ V, $V_{DDA(1V8)} = V_{DDC(1V8)} = 1.8$ V and $T_{amb} = 25$ °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clamps							
N_{CL}	clamping accuracy			-	0.1	1.8	LSB
$M_{CL(CTC)}$	channel-to-channel clamp matching			-	1.14	1.20	LSB
Phase-locked loop (PLL) of analog video part							
$t_{jit(PLL)(p-p)}$	peak-to-peak PLL jitter time	$f_s = 170$ MHz; during 3 s	[1]	-	0.16	1.60	ns
N_{pix}	number of pixels	pixels per line		256	-	4095	-
$f_{clk(ref)}$	reference clock frequency			15	-	65	kHz
$f_{clk(o)(PLL)}$	PLL output clock frequency			12.5	-	170	MHz
$\Delta\varphi$	phase difference	standard at 170 MHz		-	2.7	4.2	step
$\Delta\varphi_{step}$	phase shift step	manual controls; $T_{amb} = 25$ °C		-	11.25	-	deg
ADCs (+ AGCs)							
f_s	sampling frequency	maximum		170	-	-	MHz
INL	integral non-linearity	$f_s = 170$ MHz		-	±0.5	-	LSB
DNL	differential non-linearity	$f_s = 170$ MHz		-	±0.7	-	LSB
S/N	signal-to-noise ratio	without harmonics; $f_i = 1$ MHz; sinewave input; $f_s = 170$ MHz		-	45	-	dB
Clock timing input (CKEXT)							
$f_{clk(max)}$	maximum clock frequency			170	-	-	MHz
δ_{clk}	clock duty cycle			-	50	-	%
Clock timing output (VCLK)							
$f_{clk(max)}$	maximum clock frequency	analog inputs; RGB/YUV/YUV 4 : 2 : 2 semi-planar/ITU-R BT.656		170	-	-	MHz
δ_{clk}	clock duty cycle			45	50	55	%
Horizontal timing output (HS)							
$t_{d(pipe)}$	pipeline delay time	horizontal sync pulse delay; in phase with data outputs		-	15.4	-	clock interval
Timing output (VPA0 to VPA7, VPB0 to VPB7, VPC0 to VPC7), see Figure 10							
$t_{d(s)}$	sampling delay time	referenced to VCLK		-	3.2	-	ns
$t_{su(Q)}$	data output set-up time			-	-	4.5	ns
$t_{h(Q)}$	data output hold time			2	-	-	ns
TTL digital inputs (HCSYNC1, HCSYNC2, VSYNC1, VSYNC2 and CKEXT)							
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
I_i	input current	$V_I = 0$ V or $V_I = V_{DD}$		-	-	±5	µA
t_r	rise time	20 % to 80 %		-	-	3	ns
t_f	fall time	80 % to 20 %		-	-	3	ns

© NXP B.V. 2008. All rights reserved.

Table 58. Characteristics *...continued*

$V_{DDA(3V3)}$ = $V_{DDI(3V3)}$ = $V_{DDO(3V3)}$ = 3.15 V to 3.45 V; $V_{DDA(1V8)}$ = $V_{DDC(1V8)}$ = 1.75 V to 1.85 V; T_{amb} = 0 °C to 70 °C; typical values measured at $V_{DDA(3V3)}$ = $V_{DDI(3V3)}$ = $V_{DDO(3V3)}$ = 3.3 V, $V_{DDA(1V8)}$ = $V_{DDC(1V8)}$ = 1.8 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LV-TTL digital outputs (VPA0 to VPA7, VPB0 to VPB7, VPC0 to VPC7, VCLK, DE, HS, VS, CS, HREF, VREF, FREF)						
V_{OL}	LOW-level output voltage	V_{DDO} = 3.0 V; I_{OL} = 2 mA; C_L = 10 pF	-	-	0.4	V
V_{OH}	HIGH-level output voltage	V_{DDO} = 3.0 V; I_{OH} = –2 mA; C_L = 10 pF	2.4	-	-	V
I^2C-bus (fast-mode, 5 V tolerant; SCL and SDA)						
f_{SCL}	SCL clock frequency		-	-	400	kHz
C_b	capacitive load for each bus line		-	-	400	pF

[1] $6\sigma = 6 \times 0{,}02\text{UI} \times \frac{1}{f_s}$ Where UI = Unit Interval

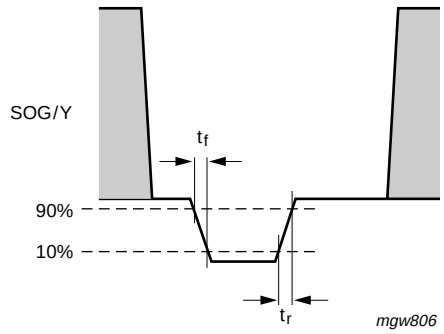


Fig 9. Horizontal sync pulse on SOG/Y

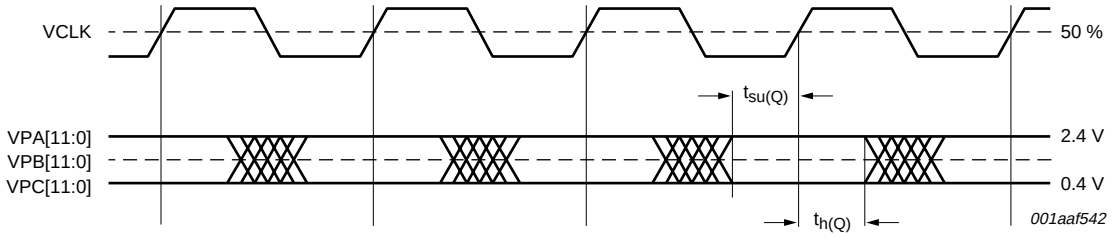


Fig 10. Output timing

© NXP B.V. 2008. All rights reserved.

Table 59. Output formats (register OUTPUT_CTRL = EAh)[1]

Signal	RGB	YUV	YUV 4 : 2 : 2 (semi-planar)		YUV 4 : 2 : 2 (ITU-R BT.656)			
VPA0	R0	V0	U0	V0	U0	$Y_0$0	V0	$Y_1$0
VPA1	R1	V1	U1	V1	U1	$Y_0$1	V1	$Y_1$1
VPA2	R2	V2	U2	V2	U2	$Y_0$2	V2	$Y_1$2
VPA3	R3	V3	U3	V3	U3	$Y_0$3	V3	$Y_1$3
VPA4	R4	V4	U4	V4	U4	$Y_0$4	V4	$Y_1$4
VPA5	R5	V5	U5	V5	U5	$Y_0$5	V5	$Y_1$5
VPA6	R6	V6	U6	V6	U6	$Y_0$6	V6	$Y_1$6
VPA7	R7	V7	U7	V7	U7	$Y_0$7	V7	$Y_1$7
VPB0	B0	U0	Z/L	Z/L	Z/L	Z/L	Z/L	Z/L
VPB1	B1	U1	Z/L	Z/L	Z/L	Z/L	Z/L	Z/L
VPB2	B2	U2	Z/L	Z/L	Z/L	Z/L	Z/L	Z/L
VPB3	B3	U3	Z/L	Z/L	Z/L	Z/L	Z/L	Z/L
VPB4	B4	U4	Z/L	Z/L	Z/L	Z/L	Z/L	Z/L
VPB5	B5	U5	Z/L	Z/L	Z/L	Z/L	Z/L	Z/L
VPB6	B6	U6	Z/L	Z/L	Z/L	Z/L	Z/L	Z/L
VPB7	B7	U7	Z/L	Z/L	Z/L	Z/L	Z/L	Z/L
VPC0	G0	Y0	$Y_0$0	$Y_1$0	Z/L	Z/L	Z/L	Z/L
VPC1	G1	Y1	$Y_0$1	$Y_1$1	Z/L	Z/L	Z/L	Z/L
VPC2	G2	Y2	$Y_0$2	$Y_1$2	Z/L	Z/L	Z/L	Z/L
VPC3	G3	Y3	$Y_0$3	$Y_1$3	Z/L	Z/L	Z/L	Z/L
VPC4	G4	Y4	$Y_0$4	$Y_1$4	Z/L	Z/L	Z/L	Z/L
VPC5	G5	Y5	$Y_0$5	$Y_1$5	Z/L	Z/L	Z/L	Z/L
VPC6	G6	Y6	$Y_0$6	$Y_1$6	Z/L	Z/L	Z/L	Z/L
VPC7	G7	Y7	$Y_0$7	$Y_1$7	Z/L	Z/L	Z/L	Z/L

[1] Z: high-impedance; L: LOW level.

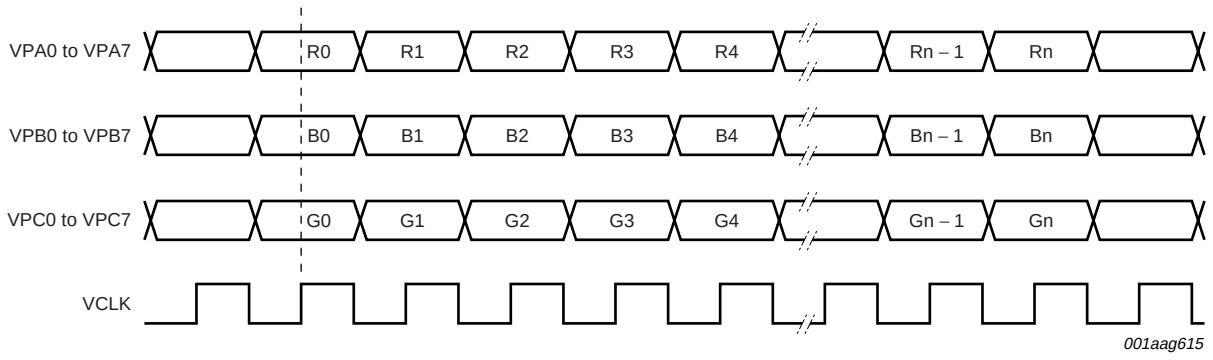


Fig 11. RGB 4 : 4 : 4 format data timing

© NXP B.V. 2008. All rights reserved.

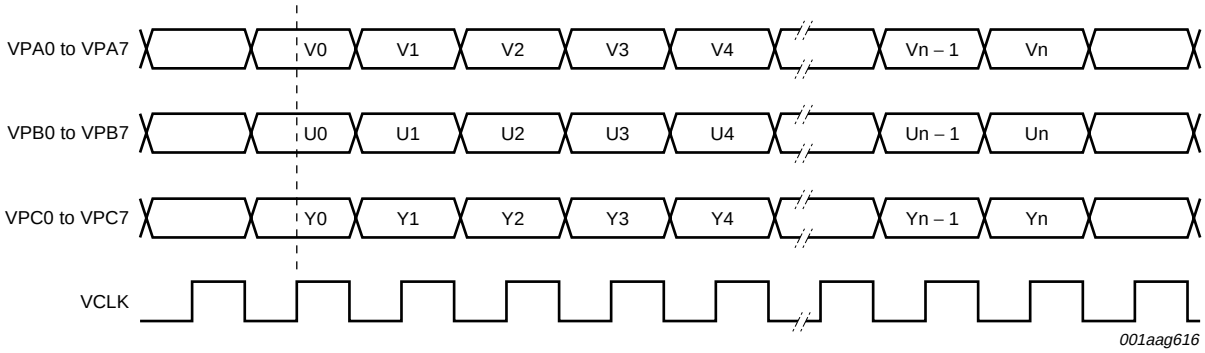


Fig 12. YUV 4 : 4 : 4 format data timing

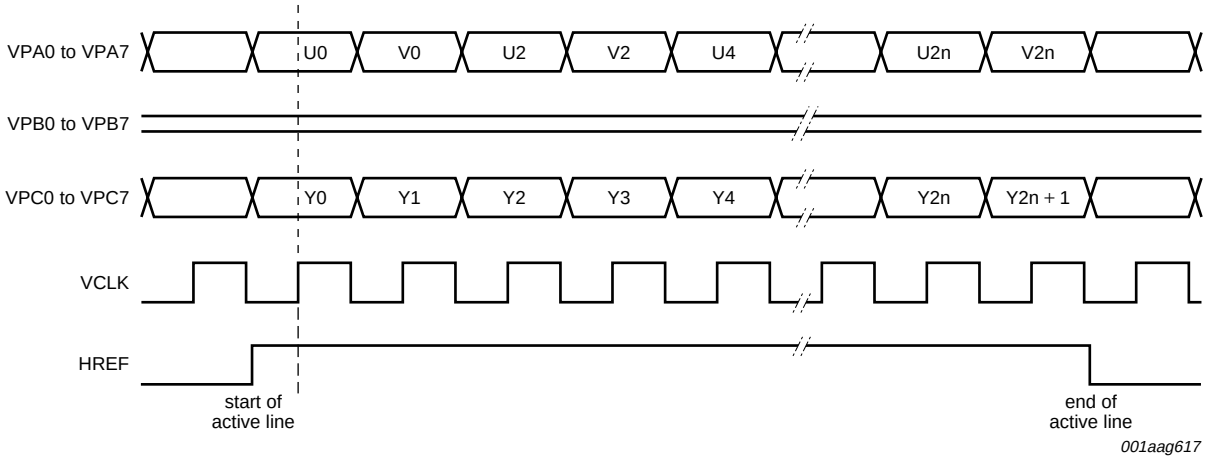
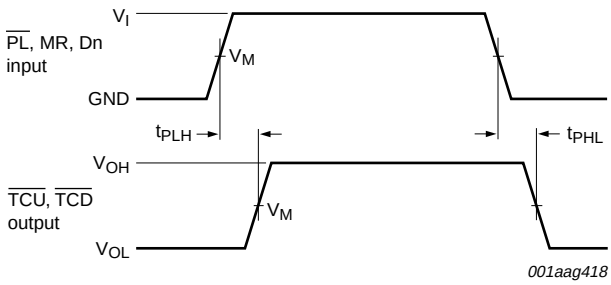


Fig 13. YUV 4 : 2 : 2 semi-planar format data timing



(1) With SAV/EAV timing codes

(2) Without SAV/EAV timing codes

Fig 14. YUV 4 : 2 : 2 ITU-R BT.656 format data timing with blanking code

© NXP B.V. 2008. All rights reserved.

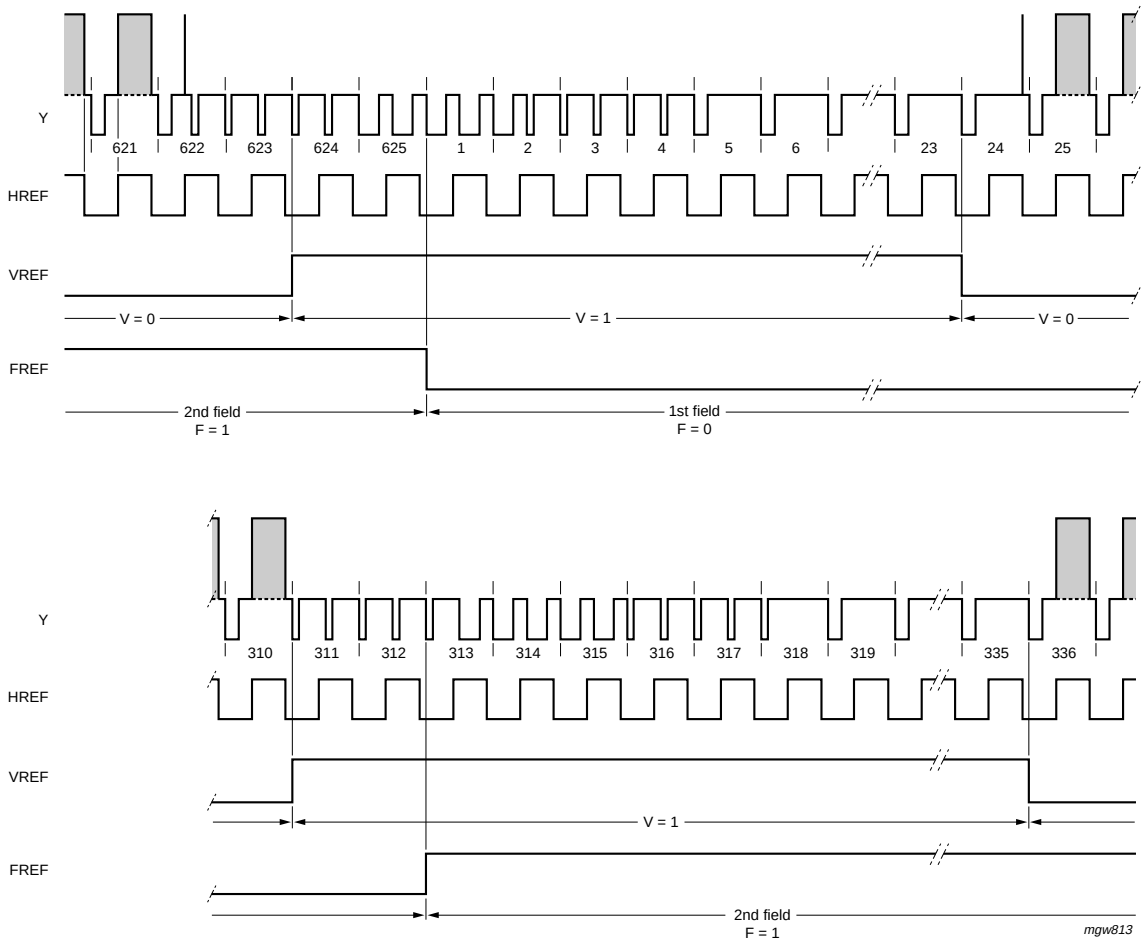


Fig 15. 576i timing in automatic mode

© NXP B.V. 2008. All rights reserved.

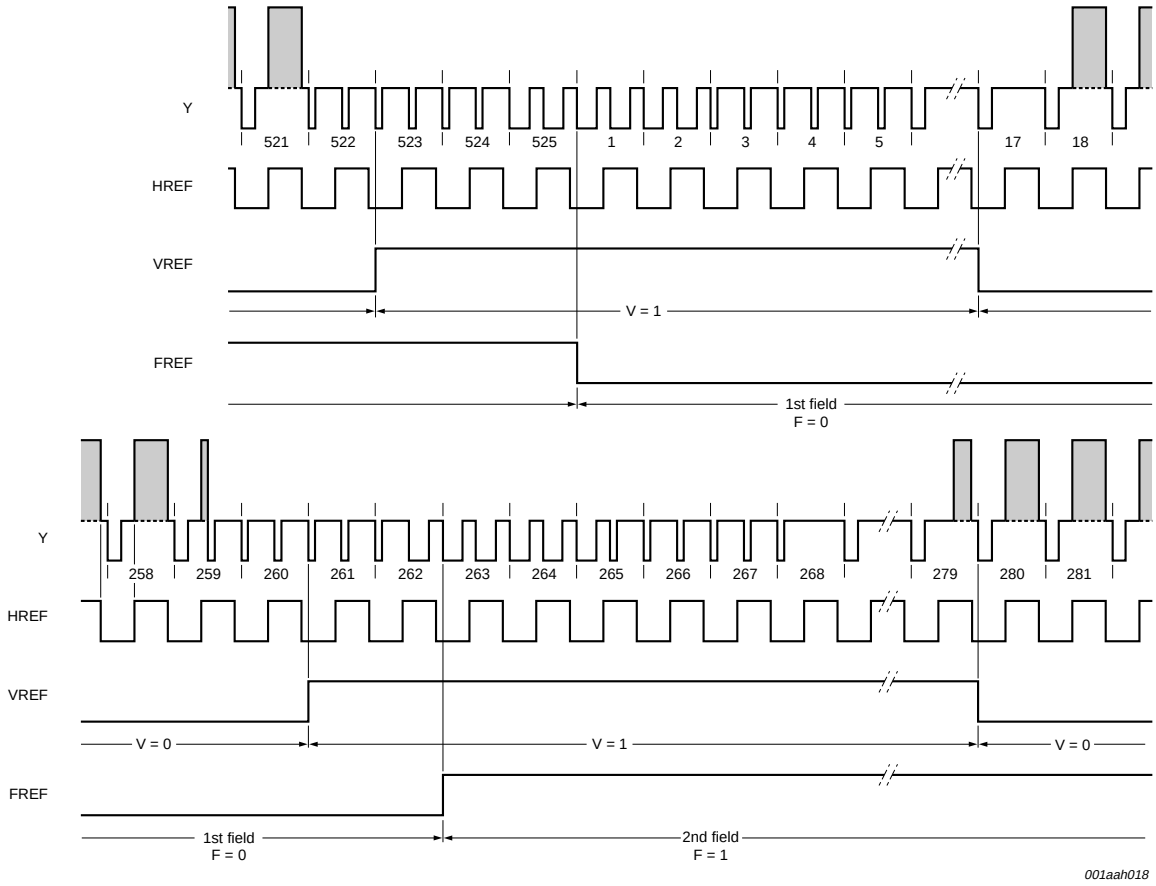
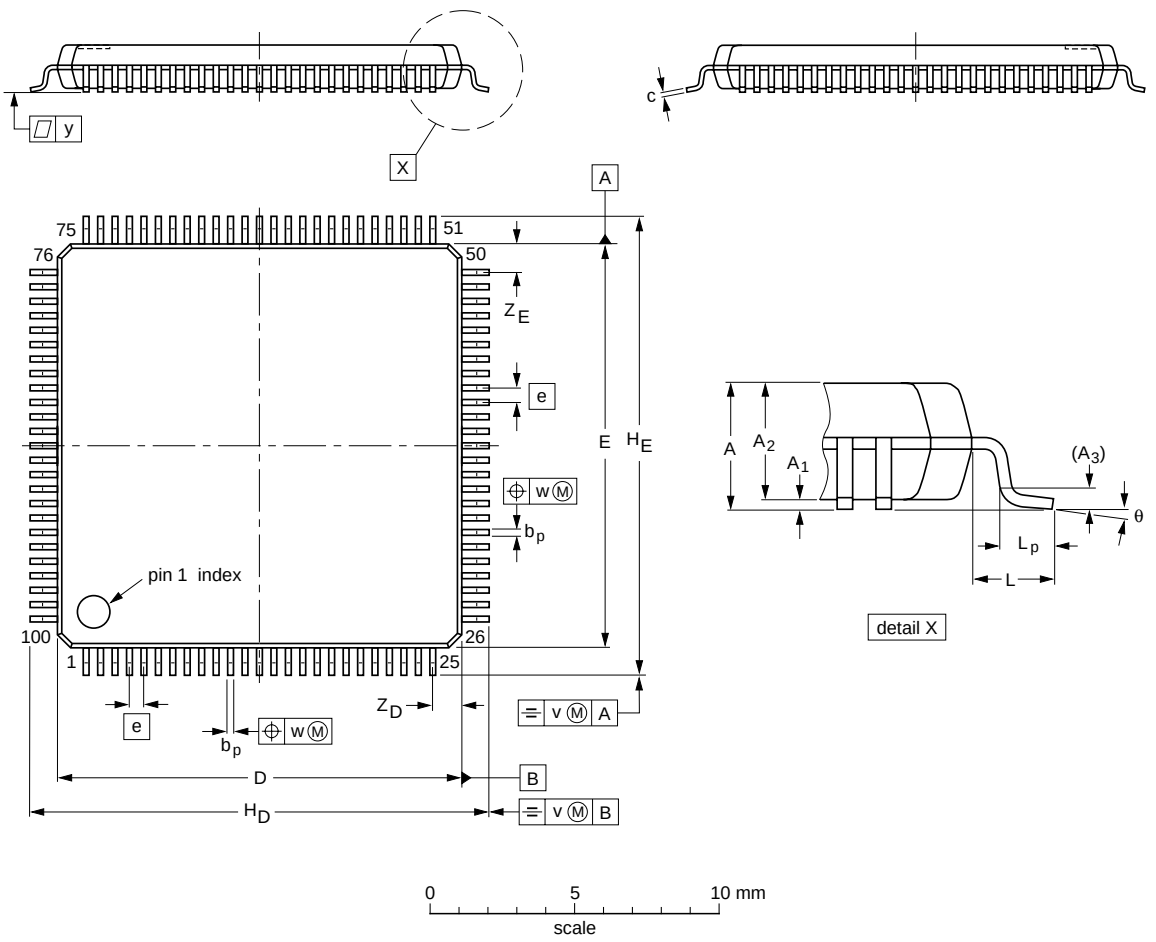


Fig 16. 480i timing in automatic mode

© NXP B.V. 2008. All rights reserved.

13. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 17. Package outline SOT407-1 (LQFP100)

© NXP B.V. 2008. All rights reserved.

14. Soldering

An in-depth account of reflow soldering can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Revision history

Table 60. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9955HL_1	20080317	Product data sheet	-	-

© NXP B.V. 2008. All rights reserved.

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I^2C-bus — logo is a trademark of NXP B.V.

17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2008. All rights reserved.

18. Contents

1 General description 1
2 Features 1
3 Applications 2
4 Ordering information 2
5 Block diagram 2
6 Functional diagram 3
7 Pinning information 4
7.1 Pinning 4
7.2 Pin description 4
8 Functional description 7
8.1 Analog multiplexers 7
8.2 R/P_R, B/P_B and G/Y channels 7
8.2.1 Clamps 7
8.2.2 ADCs 7
8.2.3 Automatic Gain Control (AGC) 7
8.3 Sync slicing 7
8.4 Activity detection 8
8.5 Sync detection and selection 8
8.6 Sync Detection Recognition and Separation . . 8
8.7 Clock generator 8
8.8 Sync multiplexers 8
8.9 Color conversion 9
8.10 4 : 2 : 2 downsample filters 9
8.11 Range control 9
8.12 4 : 2 : 2 formatter 9
8.13 Video port selection 10
8.14 Output buffers 10
8.15 VHREF timing generator 10
8.16 I^2C-bus serial interface 10
8.17 Power management 10
8.18 Sync timing measurement 10
9 I^2C-bus interface 10
9.1 I^2C-bus protocol 10
9.2 Registers definitions 11
9.2.1 Version register 17
9.2.2 Input selection register 17
9.2.3 Sync detection recognition and separation registers 17
9.2.4 PLL registers 18
9.2.5 Pixel clocks generation registers 19
9.2.6 Pixel clocks generation registers 21
9.2.7 Clamp levels registers 22
9.2.8 Video gain registers (GAIN_RV, GAIN_BU, GAIN_GY) 22
9.2.9 Sync timing measurement registers 23
9.2.10 Color space conversion registers 24
9.2.11 Line and pixel counters 26
9.2.12 Prefiltering register (PRE_FILTERS) 34
9.2.13 Range control registers 34
9.2.14 Output formatter register 35
9.2.15 Sync output selection registers 36
9.2.16 Output polarity control register 36
9.2.17 Video ports control register 37
9.2.18 Data enable signal control register 37
9.2.19 Software reset registers 38
9.2.20 Power-down control registers 39
10 Limiting values 41
11 Thermal characteristics 41
12 Characteristics 42
13 Package outline 49
14 Soldering 50
15 Revision history 50
16 Legal information 51
16.1 Data sheet status 51
16.2 Definitions 51
16.3 Disclaimers 51
16.4 Trademarks 51
17 Contact information 51
18 Contents 52

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2008. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 17 March 2008
Document identifier: TDA9955HL_1

founded by

PHILIPS